REATISS

MASTERING RE ON MODERN CHIPS

ESSENTIAL MILESTONES
Practical Recommendations

REATISS brief Introduction

- We started Reverse Engineering 26 years ago**.** Our team based in Kyiv, Ukraine started exclusive commercial RE services for Motorola and very soon under name ISS became an official vendor of Motorola and later - a primary vendor for Freescale Semiconductor Inc.
- In Y2015, after re-branding as REATISS we started open market operations with a team of 60 engineers
- Our clients are US based major semiconductor manufacturers, patent owners and law firms in US and EU. We provide solid technical evidence of use (EoU) of Client's IP in products of other companies.
- In Y2022 REATISS adjusted organizational boundaries and continues providing reverse engineering services without interruptions in difficult circumstances in Ukraine this year.

REATISS brief Introduction, cont.
Technical Areas of Expertise

Semiconductor Products

- DRAM, SRAM, Flash, EEPROM, etc.
- MCU, SoC, Processor
- Image capture devices
- MEMS

Consumer Devices

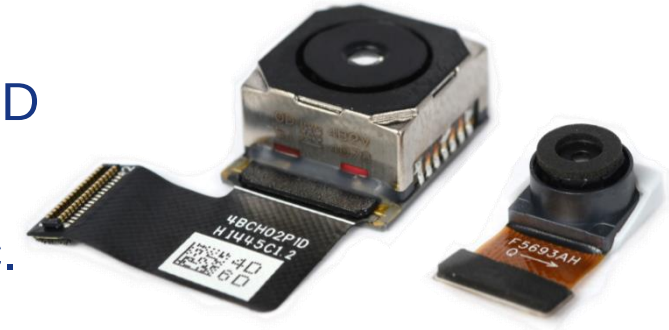
- Smartphone, Tablet, Digital Camera,
- HDD, SSD, TV, Game System, etc.

IC Technologies

- Bipolar, CMOS, FinFET, Tri-Gate, AMOLED

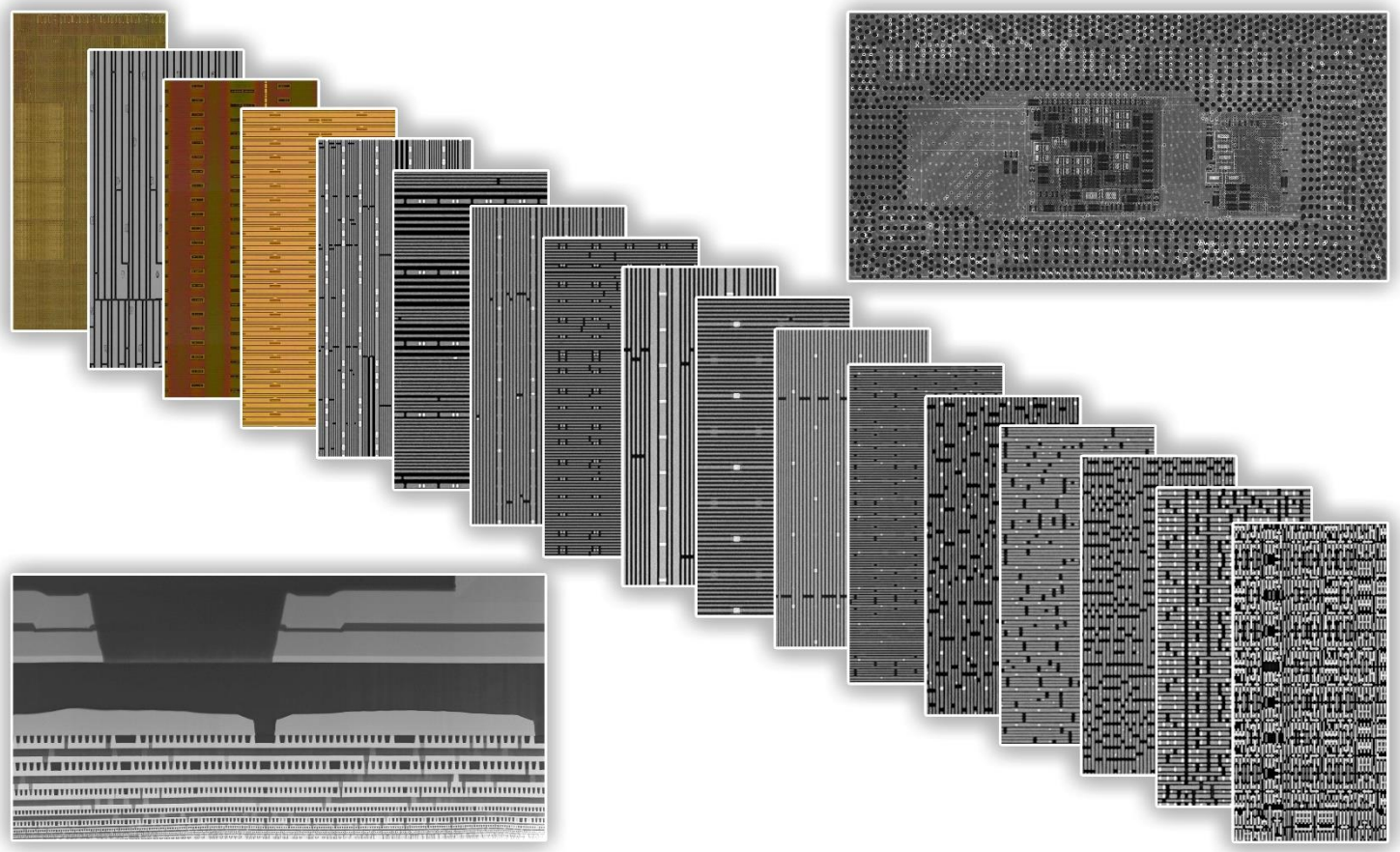
Wireless Technologies

- WiFi, Bluetooth, FM, LTE, GPS, NFC, etc.



ESSENTIAL MILESTONES

- Sample preparation, process analysis
- Imaging, distortion compensation
- Multilayer visualization of the die, horizontal and vertical synchronization of huge digital maps of all layers, easy and fast zoom in, zoom out, annotation
- Circuitry extraction and analysis, patent claim mapping
- Online access to interactive image Data Base



Essential of Sample Preparation

- Our analytical lab uses rather standard equipment for sample preparation: Allied polishing machines, Oxford RIE Plasma Etcher, Modern JEOL SEM for inspection, coaters and other minor tools and common chemical lab equipment.

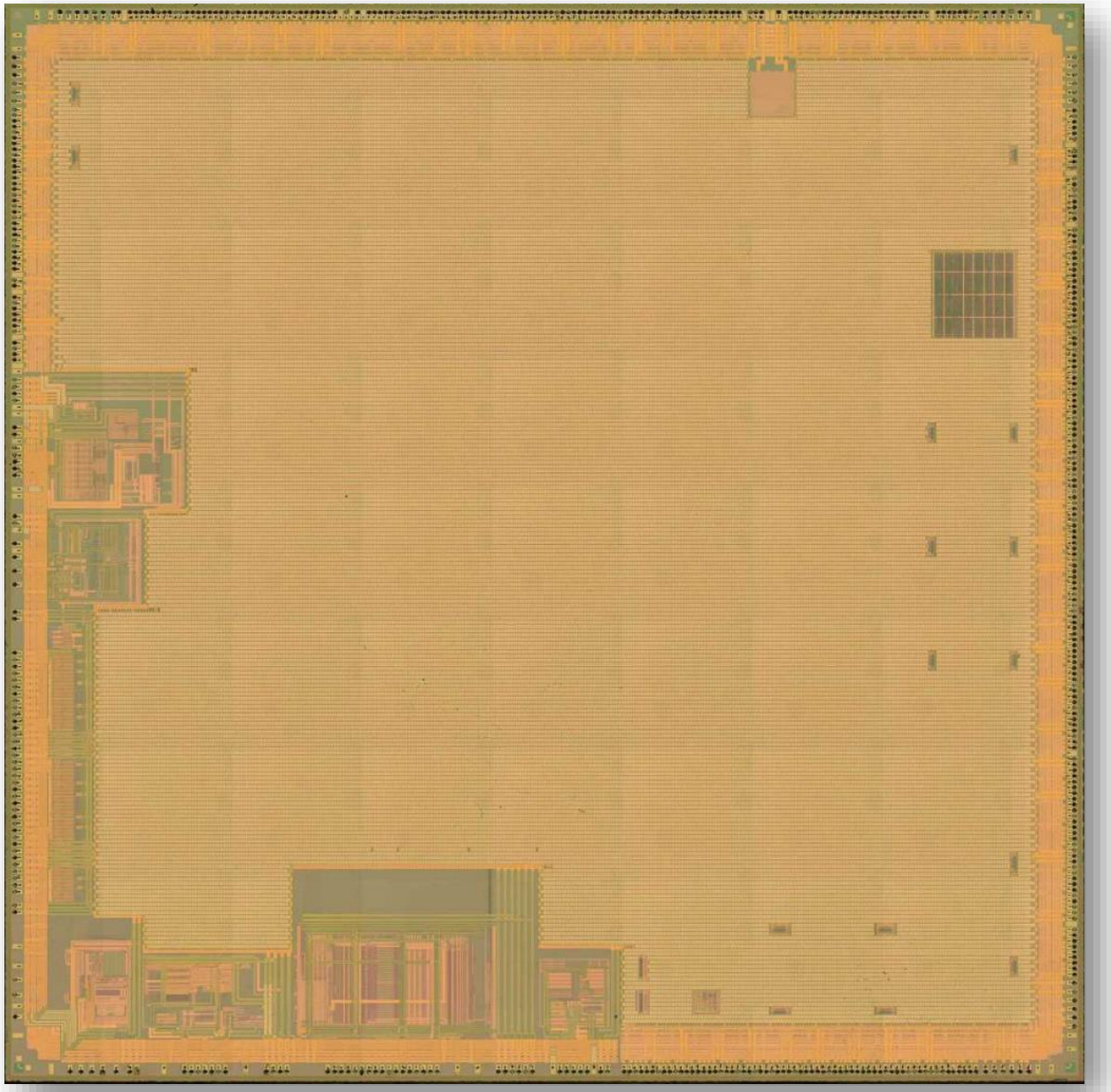
- ESSENTIAL are skills of the engineers!
- Our junior engineers are admitted to do sample prep operations after two years of daily supervised practice at workplace

- On next slides see examples of the sample prep for the whole planar die with 180 nm technology and big areas of FinFET 5 nm die

Controller, Whole Die Layout, Technology 180 nm

- Die size: 9.4 x 9.4 mm
- Total Metal Layers: 7

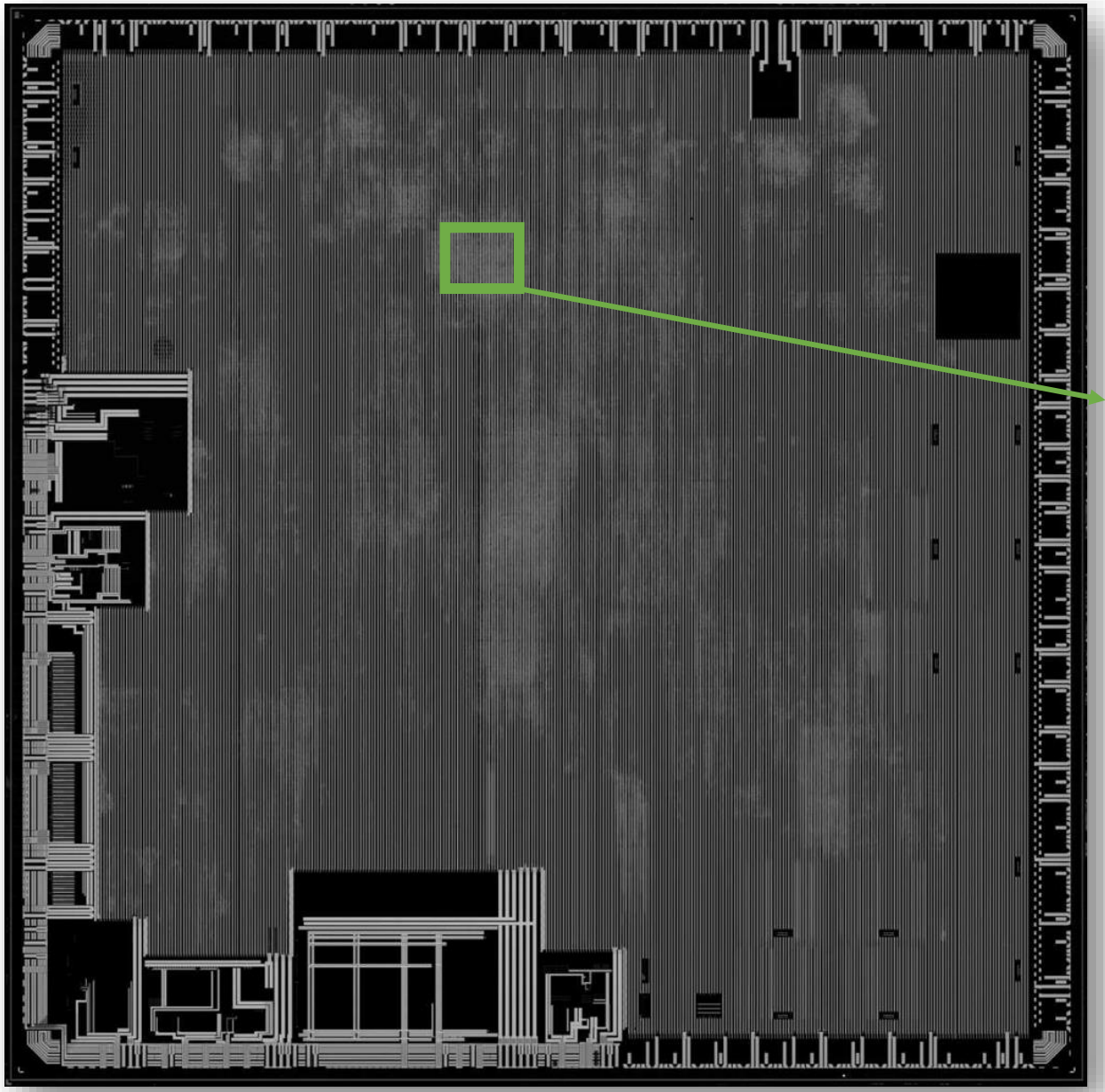
- Timeline for Layout: 11 weeks



Metal Layer 7

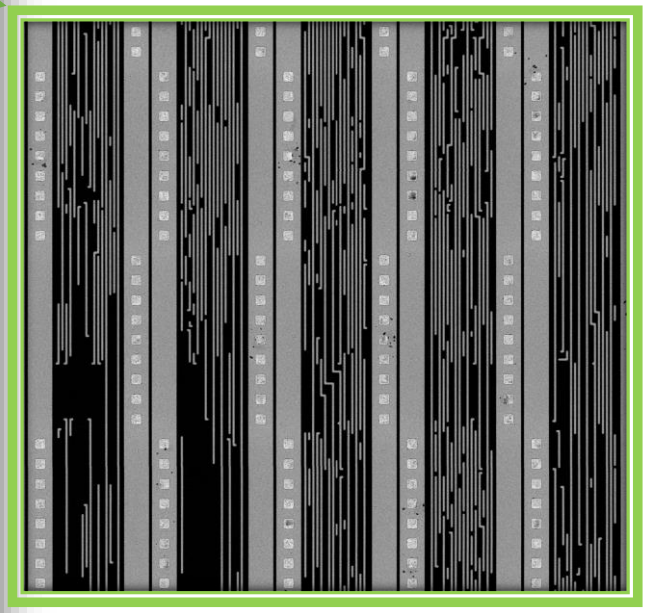
Controller, Whole Die Layout, Technology 180 nm

- Die size: 9.4 x 9.4 mm
- Total Metal Layers: 7



Metal Layer 6

Zoom In



Controller, Whole Die Layout, Technology 180 nm

- Die size: 9.4 x 9.4 mm
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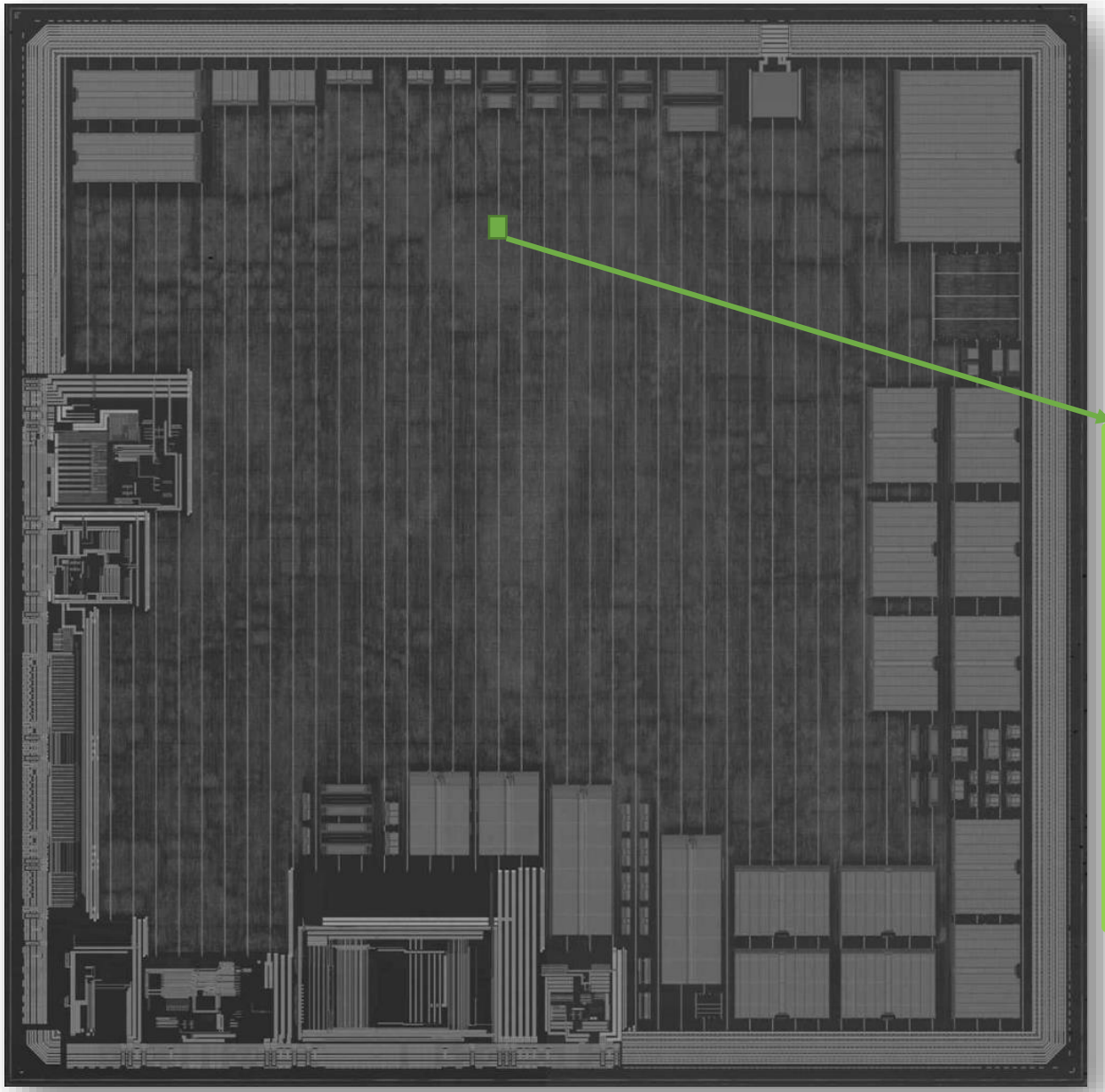
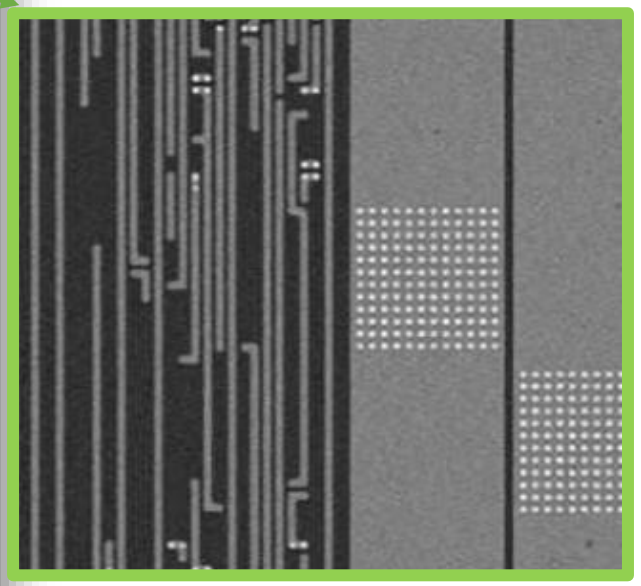


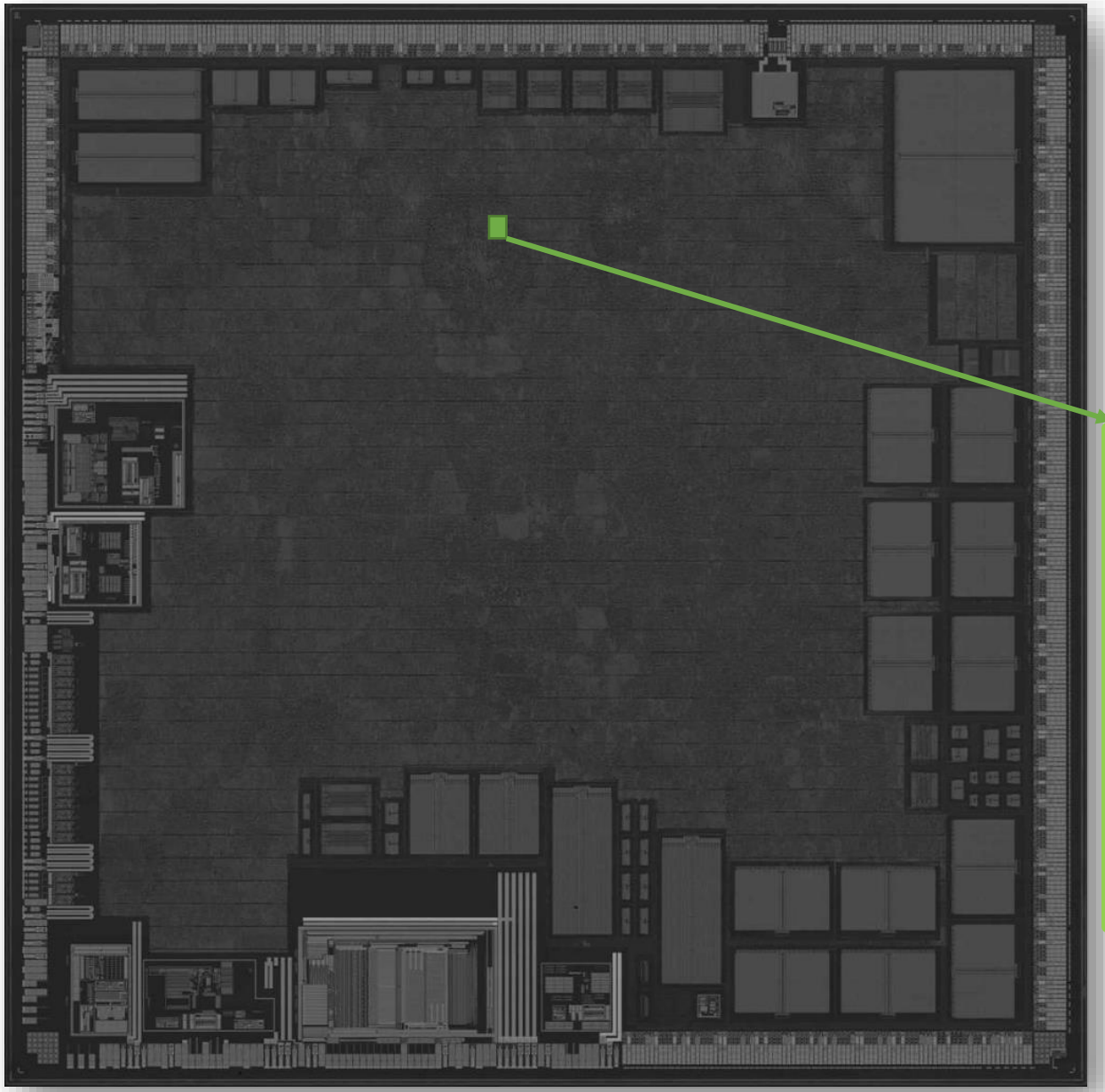
Metal Layer 4

Zoom In



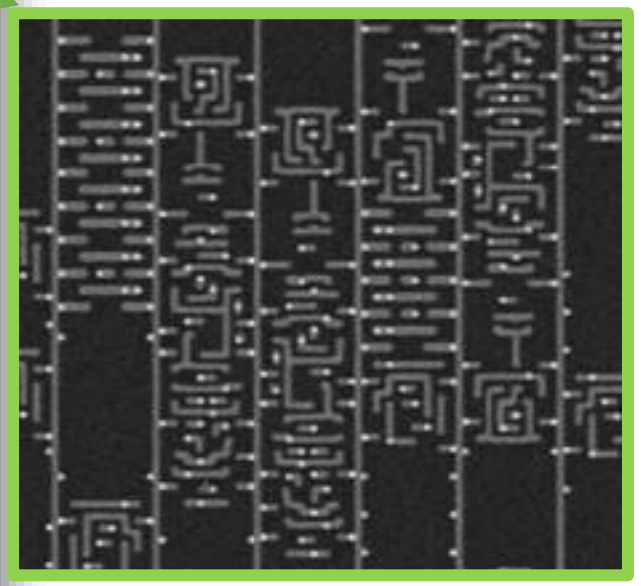
Controller, Whole Die Layout, Technology 180 nm

- Die size: 9.4 x 9.4 mm
- Total Metal Layers: 7



Metal Layer 1

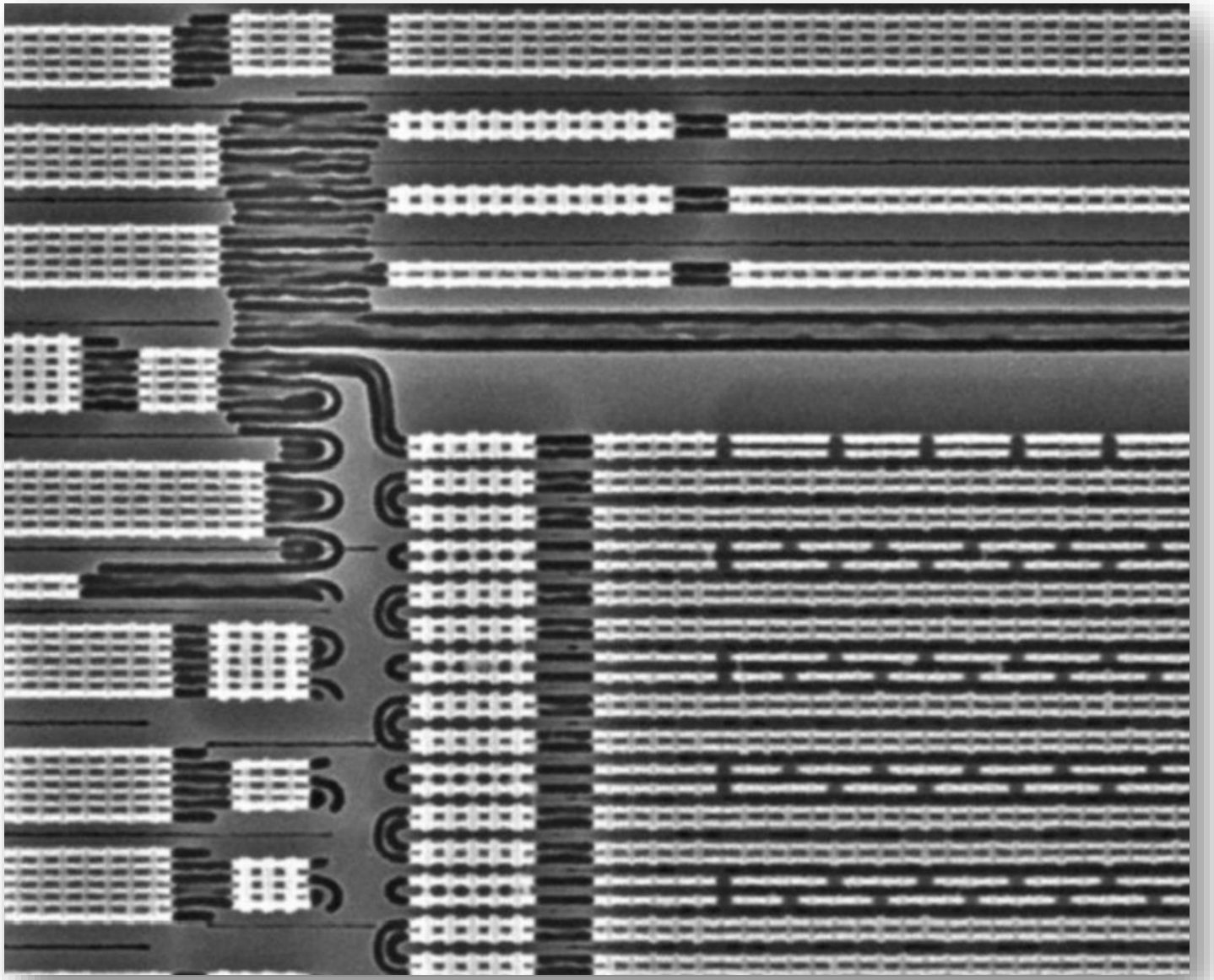
Zoom In



SoC, FinFET, technology 5 nm

- SoC, FinFET, 5 nm
- Metal Layers: 16

Focused Layout and Extraction, 1300 schematic pages of various IP blocks, Y2021, timeline: 6 months

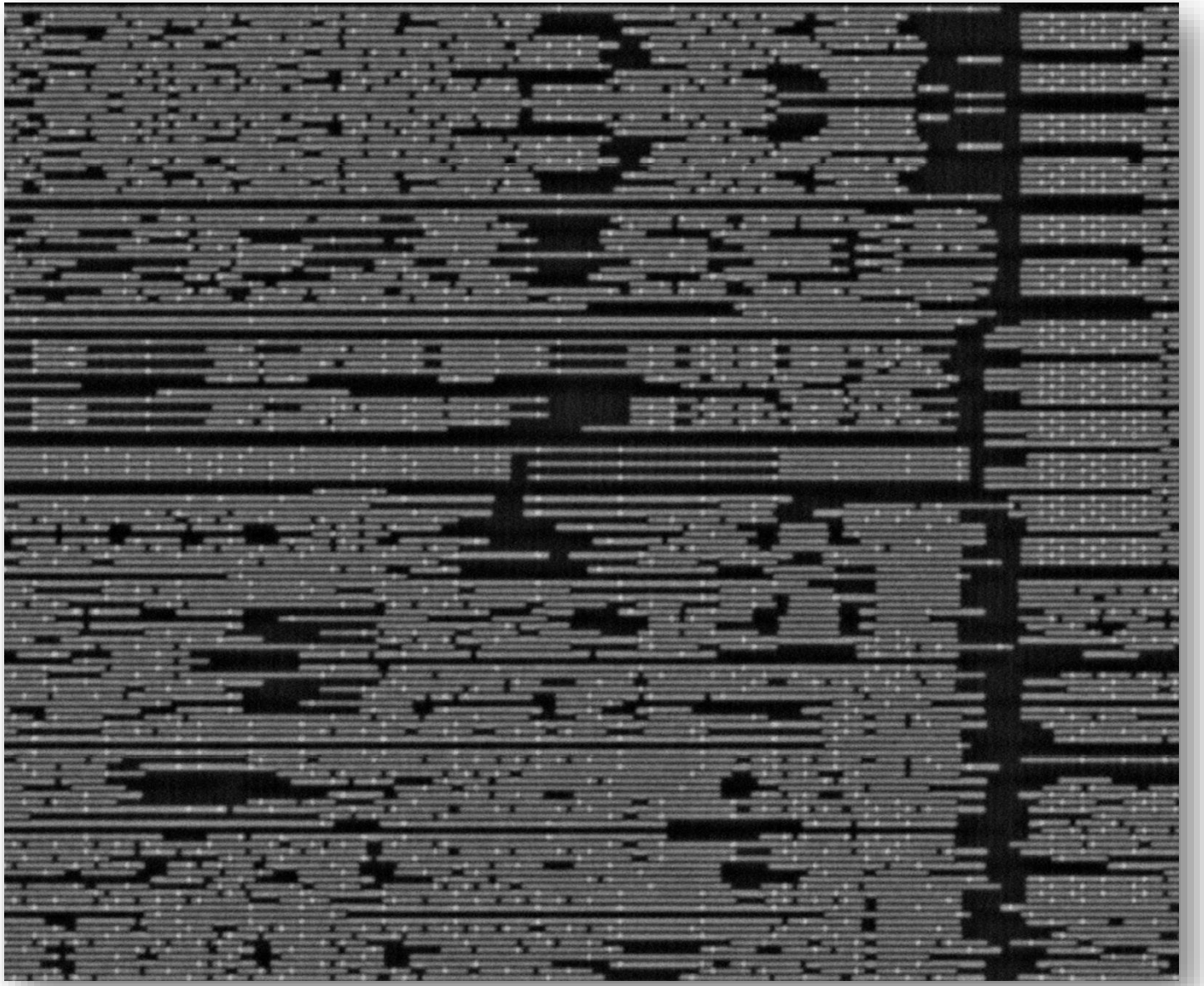


Fins, SRAM

SoC, FinFET, technology 5 nm

- SoC, FinFET, 5 nm
- Metal Layers: 16

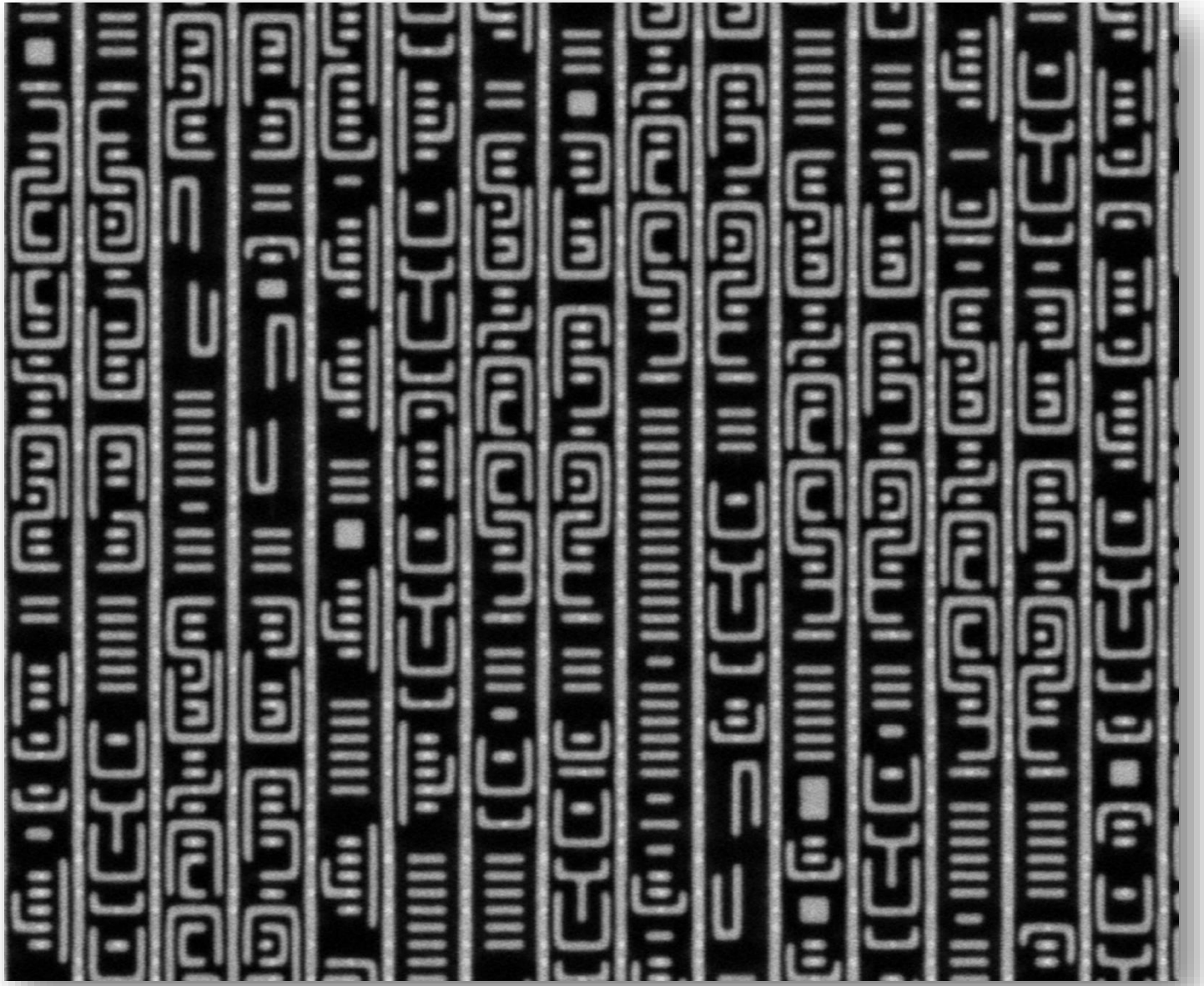
Focused Layout and Extraction, 1300 schematic pages of various IP blocks, Y2021, timeline: 6 months



M1, SRAM

Mobile Processor, FinFET, Technology 5 nm

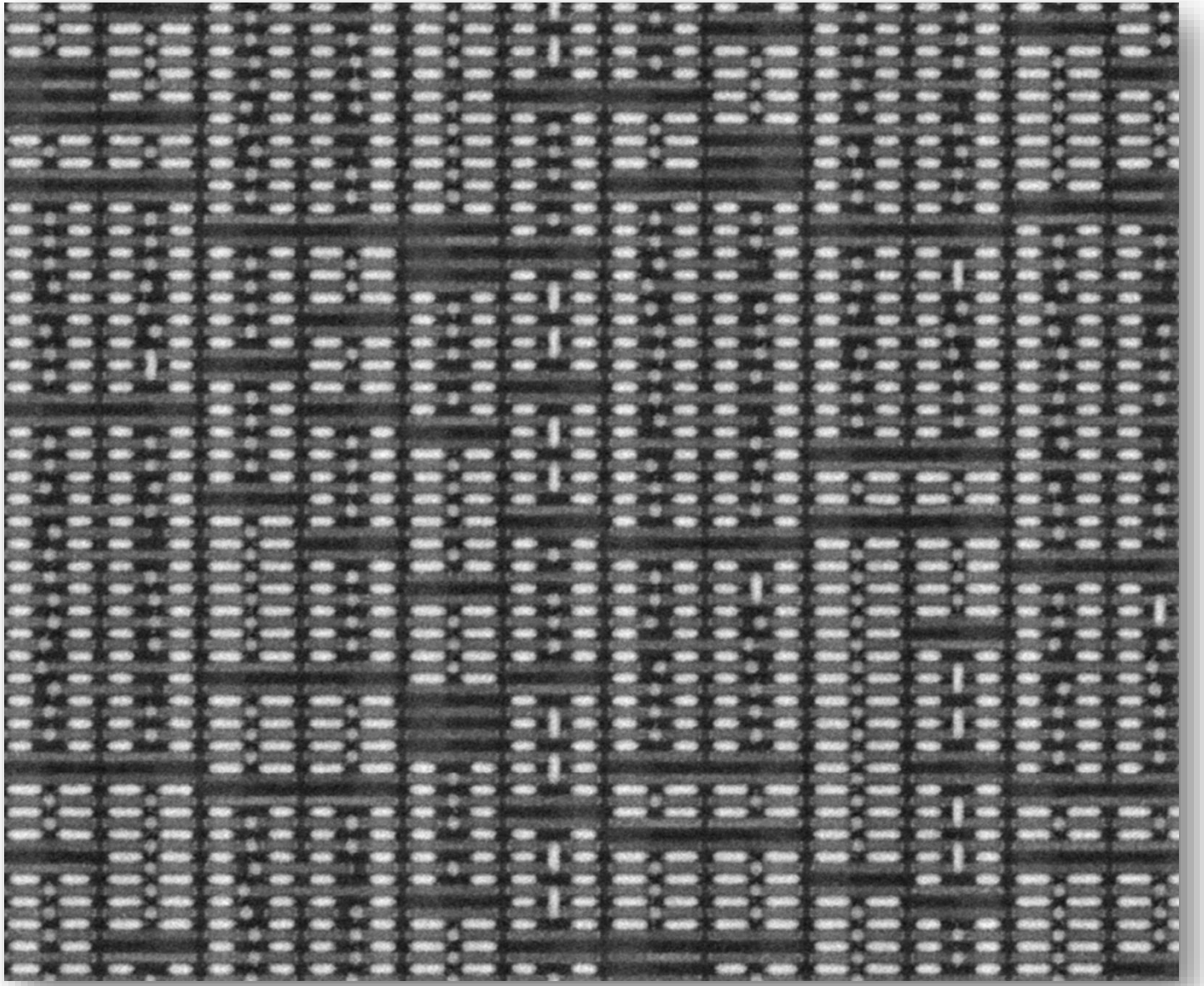
- FinFET, 5 nm
- Metal Layers: 14



M1 Logic Area

Mobile Processor, FinFET, Technology 5 nm

- FinFET, 5 nm
- Metal Layers: 14



Gates,
Logic Area

Essential Conditions for Huge Digital Die Maps Generation

- Visualization of multiple physical layers of the die in digital form requires both special imaging equipment and sophisticated digital processing including distortions compensations followed by stitching of thousands images in huge digital maps with highest accuracy.

- For many years we use RAITH Chipscanner Two with AsB detector for imaging due to its highly precise piezo moving stage, laser navigation and high accuracy of image frames, high stability of parameters during long hours of imaging session, initial automated stitching capability, low voltage of the SEM column is appropriate for the tiny semiconductor structures.

- Those features allow to keep good stability of the selected parameters of imaging like contrast, focus, brightness during many hours of imaging of big areas.

- Recent Zeiss Multi-SEM tool provides very fast scanning on big die areas therefore stability of SEM parameters should be guaranteed during image session. So, this tool may have high potential for fast imaging of big areas and have perspectives for certain RE tasks.

Essential Conditions of Huge Digital Die Maps Generation, cont.

- Even when high accuracy equipment is used for imaging, one can still observe certain remaining distortions of different nature. Such remaining distortions and scaling fluctuations require sophisticated postprocessing of obtained images enabling stitching with high accuracy especially on the dice that have no suitable refer points, e.g., big areas of repeatable dummy features.

- Our in-house developed techniques for distortion compensation and high accuracy stitching methods allow to obtain accurate multilayers digital maps of the die in all layers synchronized horizontally and vertically with accuracy 1pixel. Such multilayer digital maps are in our Data Base and are accessible online from PC or Smartphone.

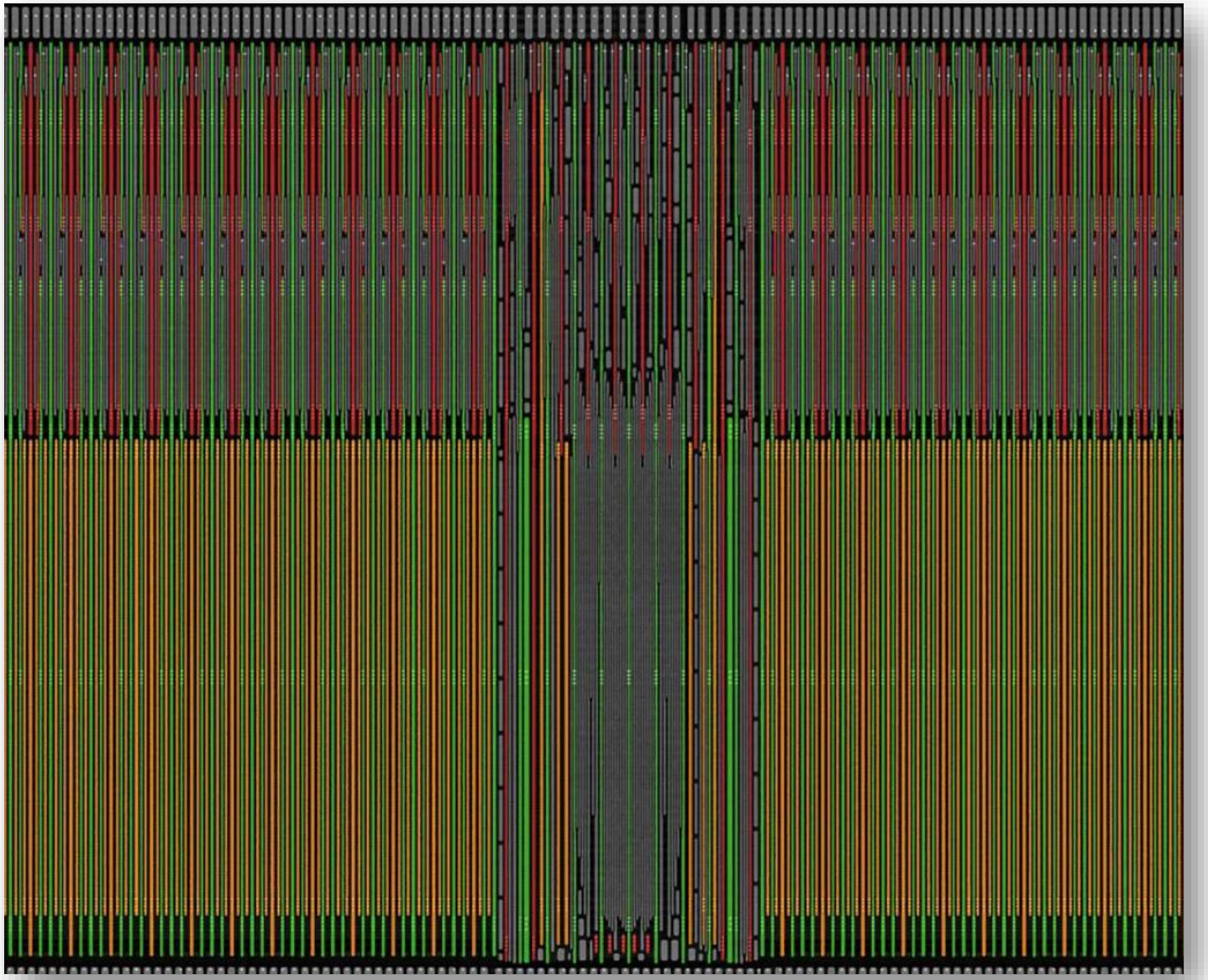
- When RE of modern chips is provided for customers, it is important to find a balance between quality, time and price at given scope. It seems easier to use higher magnification and apply standard automated image recognition and get high quality results, however in case for modern chips with 5 nm technology the time and price will jump up considerably. Especial critical parameter is a time, as clients may have solid deadlines in litigation process. So, it always should be found a reasonable mix of human skills and automation tools.

- Next slides demonstrate automatically vectorized buses on the die and stitched image

SoC, FinFET, Technology 5 nm

- SoC, FinFET, 5 nm
- Metal Layers: 16

Automatically Recognized
Selected Buses and Vias

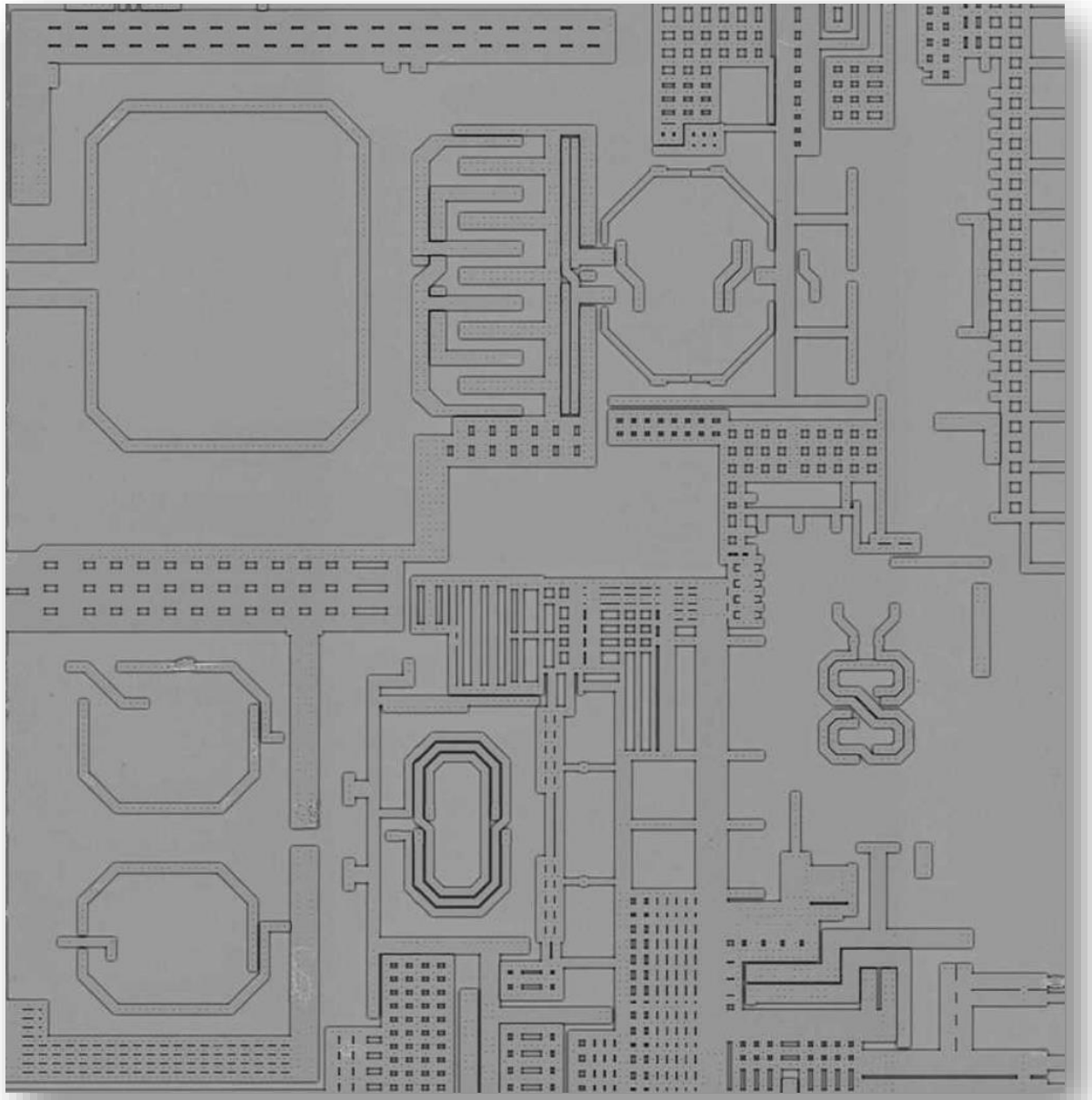


M5, SRAM

WLAN Controller, Technology 32 nm

- WLAN Controller, 32 nm
- Metal Layers: 7

Focused Layout and Extraction,
100 schematic pages,
timeline: 3 months

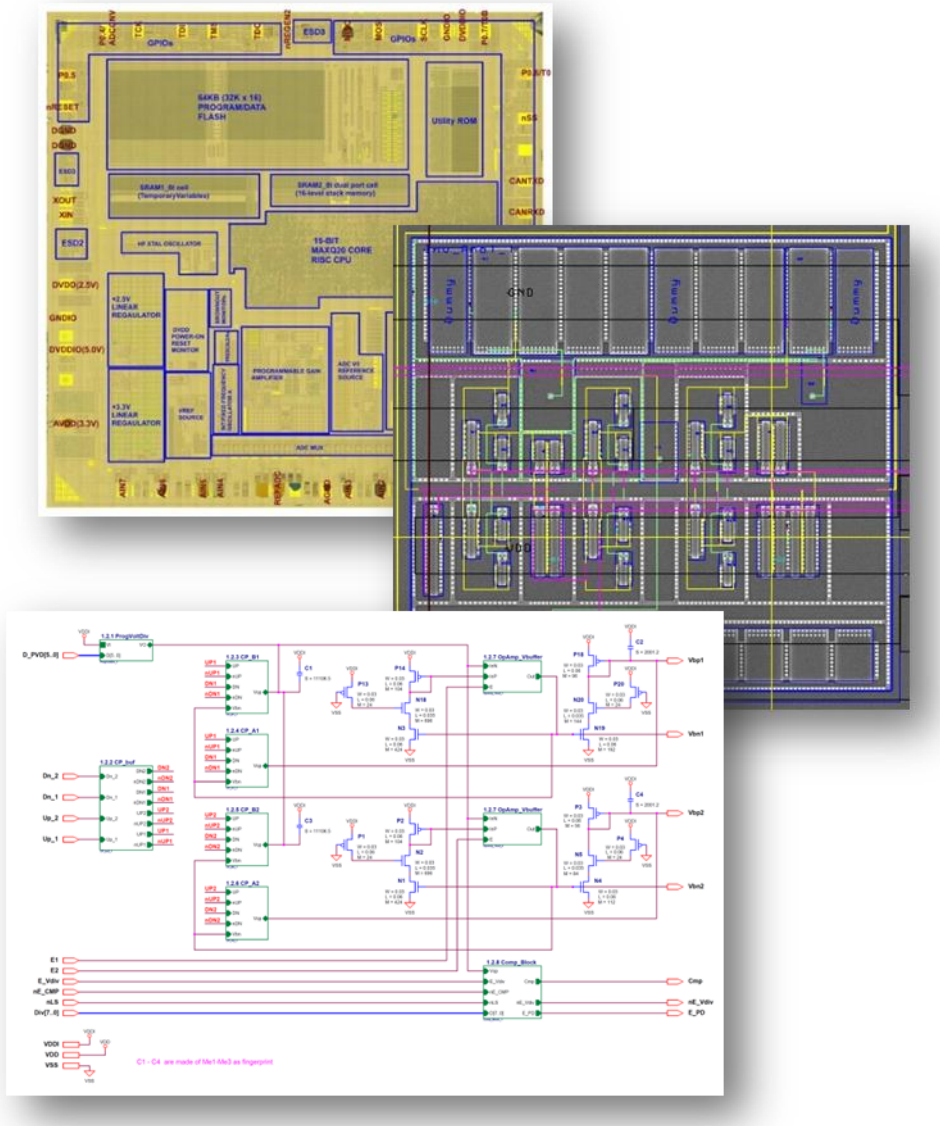


Metal Layer 7

Essential of Circuitry Extraction and Analysis

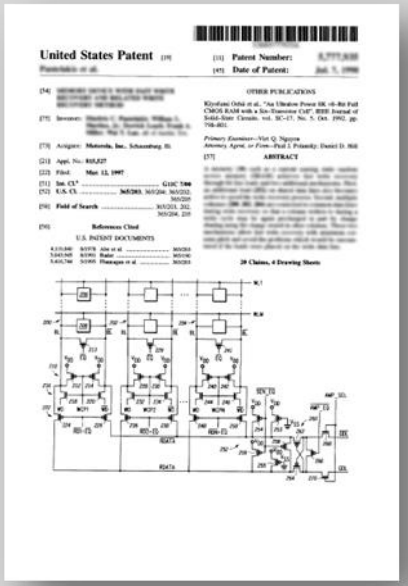
Circuitry extraction of modern chips requires automated tools. We use our in-house developed software tool to trace and extract circuitry to help our experts in performing circuitry analysis.

Hierarchically organized reports have convenient navigation system that helps to detect quickly and comprehensively the evidences of patents infringements.

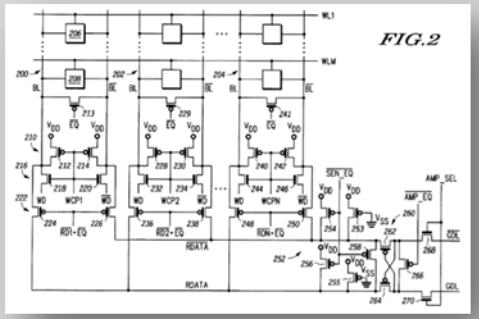


Patent Infringements Analysis and Claim Mapping

- Solid technical evidences of patent Infringements found at RE process support our clients in their IP protection and monetization, licensing, patent trade and litigation
- Here goes example of claim mapping that proves patent infringement based on results of physical RE as was demonstrated above in all aspects



Step 1. Perspective Patent Selection



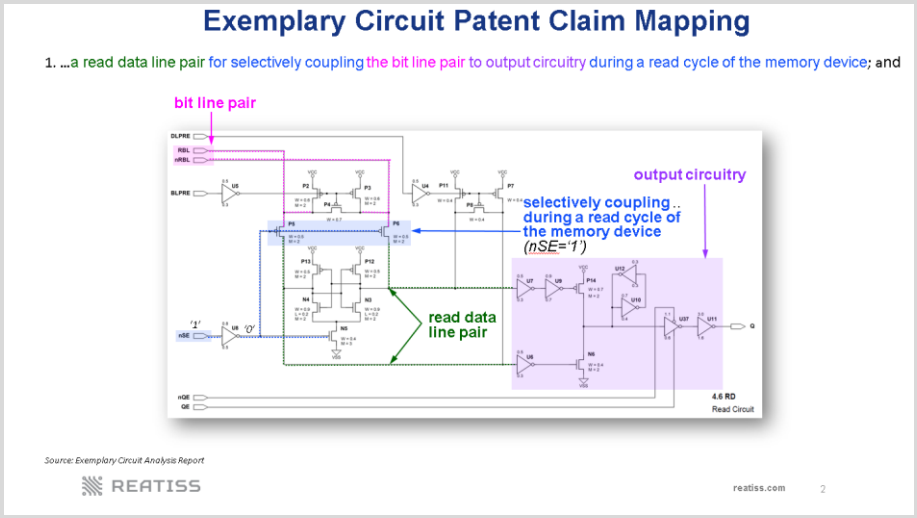
1. A memory device, comprising:

a plurality of memory cells, each memory cell of the plurality of memory cells coupled to a word line and to a bit line pair;

a bit line load, coupled to the bit line pair, for charging the bit line pair to a predetermined voltage in response to a first control signal;

a read data line pair for selectively coupling the bit line pair to output circuitry during a read cycle of the memory device; and

Step 2. Claims Analysis



Step 3. Mapping claims elements to evidences of use

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Thank you!