Open Source T&M for Hardware RE

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IOActive
Hardware | Software | Wetware
SECURITY SERVICES

The Problem

- Digital interfaces are getting faster
  - Probing is getting harder and more expensive
- Protocol stacks are growing in complexity
  - Need more decodes to understand behavior
  - Need extensibility for emerging or proprietary protocols
- Closed source implementations are problematic
  - $$$$
  - Hard to extend, modify, etc. RE needs adaptability

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The Solution: Open T&M Platform

- Distant descendent of internal tooling for my Ph.D
- Now released as open source
  - Used internally at IOA, but not “our” project
  - They paid for my travel so get credit on the slides ☺
- Industry adoption and support is growing
- Healthy, growing community userbase

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Probing Suite

- Excellent cost / performance ratio
- Vendor independent interface
- All models so far are solder-in for extended probing
  - Optimized for RE use case of many long captures
  - Handheld browser versions may come eventually

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Probing Suite

- Designs are on GitHub now for early adopters to DIY
- Working on plans for production runs later this year

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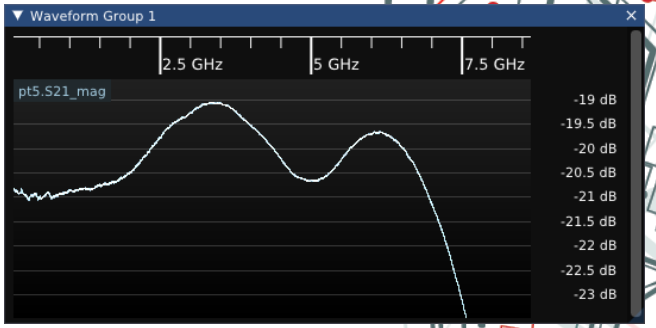
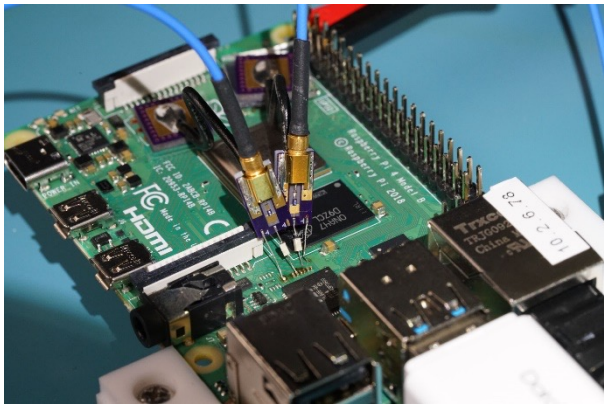
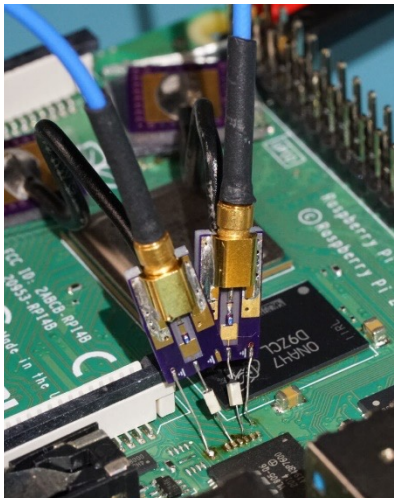
AKL-PT5

https://github.com/azonenberg/starshipraider/tree/master/boards/probes/akl-pt5



- 7.5 GHz -3 dB BW (w/ cable de-embedded)
- 500Ω 10:1 DC coupled transmission line probe
- Suitable for decodes of PCIe gen3, USB3, 10Gbase-R





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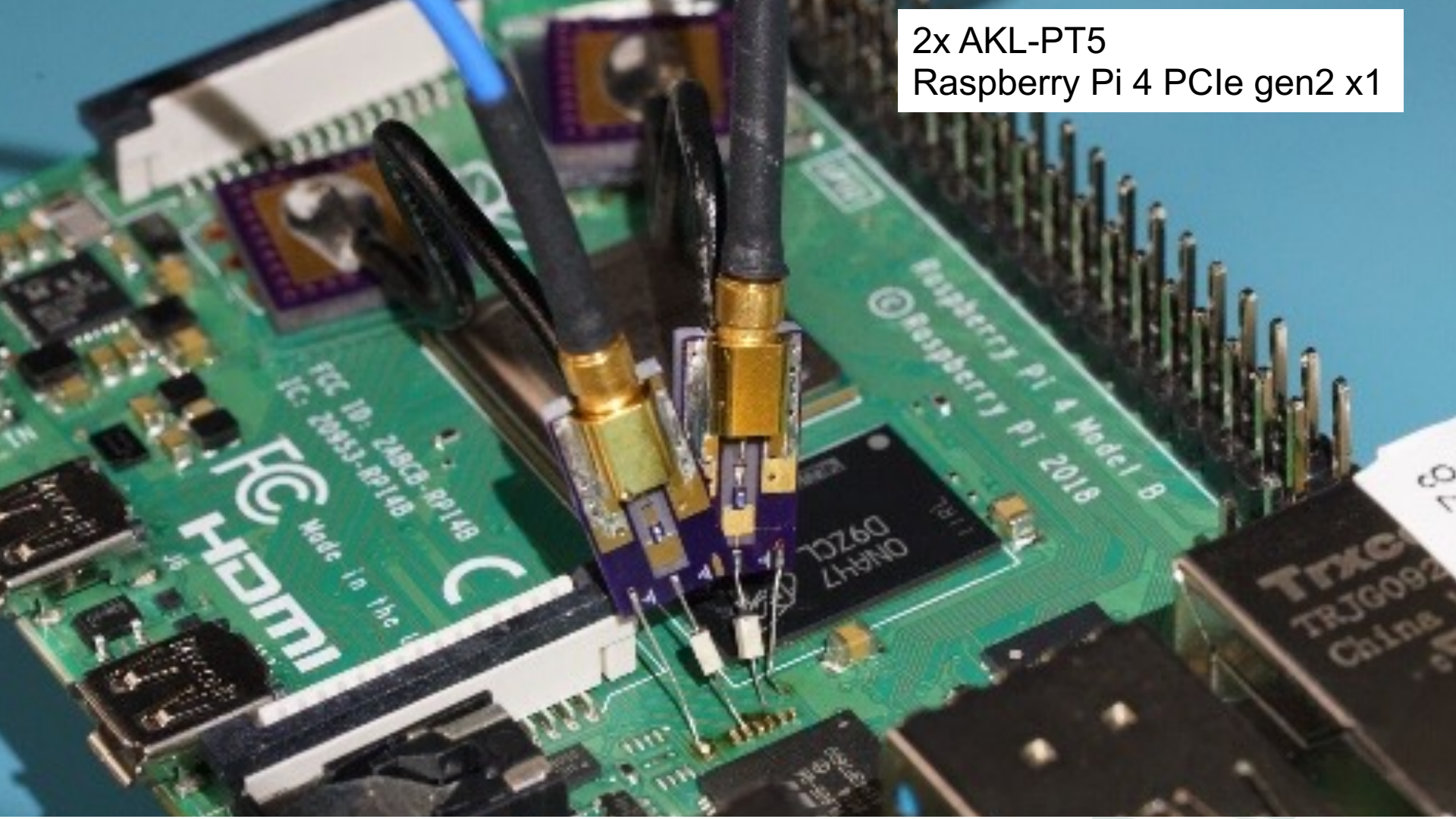
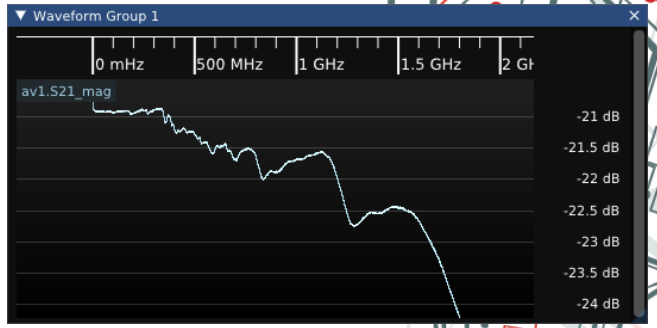
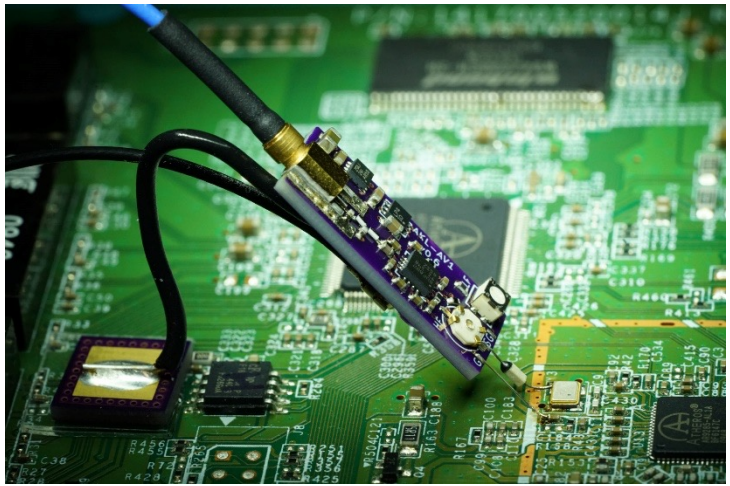

2x AKL-PT5
Raspberry Pi 4 PCIe gen2 x1

AKL-AV1

https://github.com/azonenberg/starshipraider/tree/master/boards/probes/akl-av1

- 1.75 GHz 10:1 high impedance voltage probe
- 5MΩ || 350 fF input
- Great for weak, loading-sensitive signals





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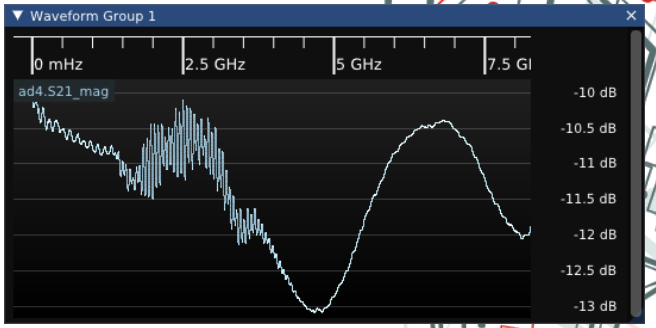
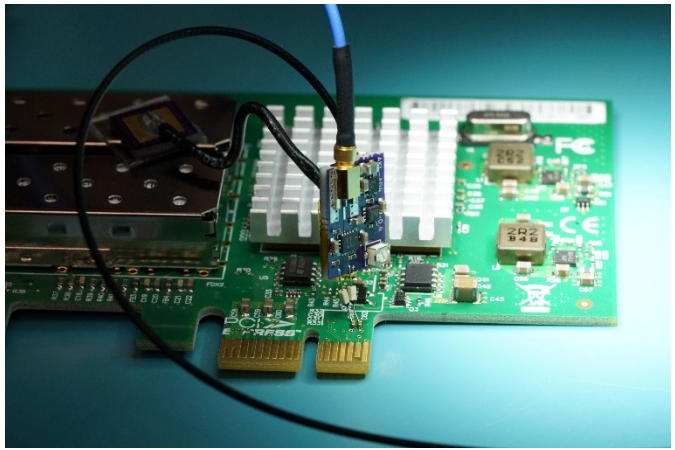
AKL-AV1
Crystal oscillator on router

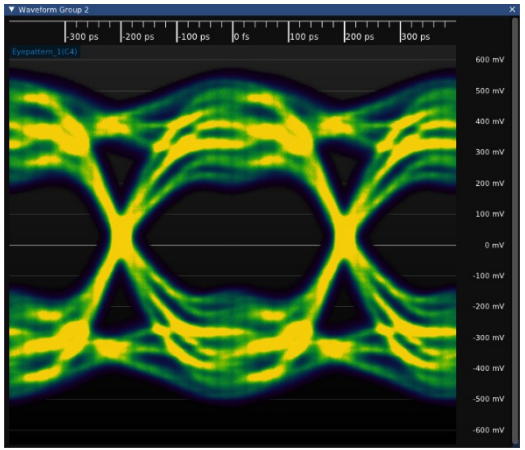
AKL-AD4

https://github.com/azonenberg/starshipraider/tree/master/boards/probes/akl-ad4



- >8 GHz low impedance active diff probe
- Resistive input, 500Ω to ground from each leg
- Two PT5 style inputs feeding a differential amplifier





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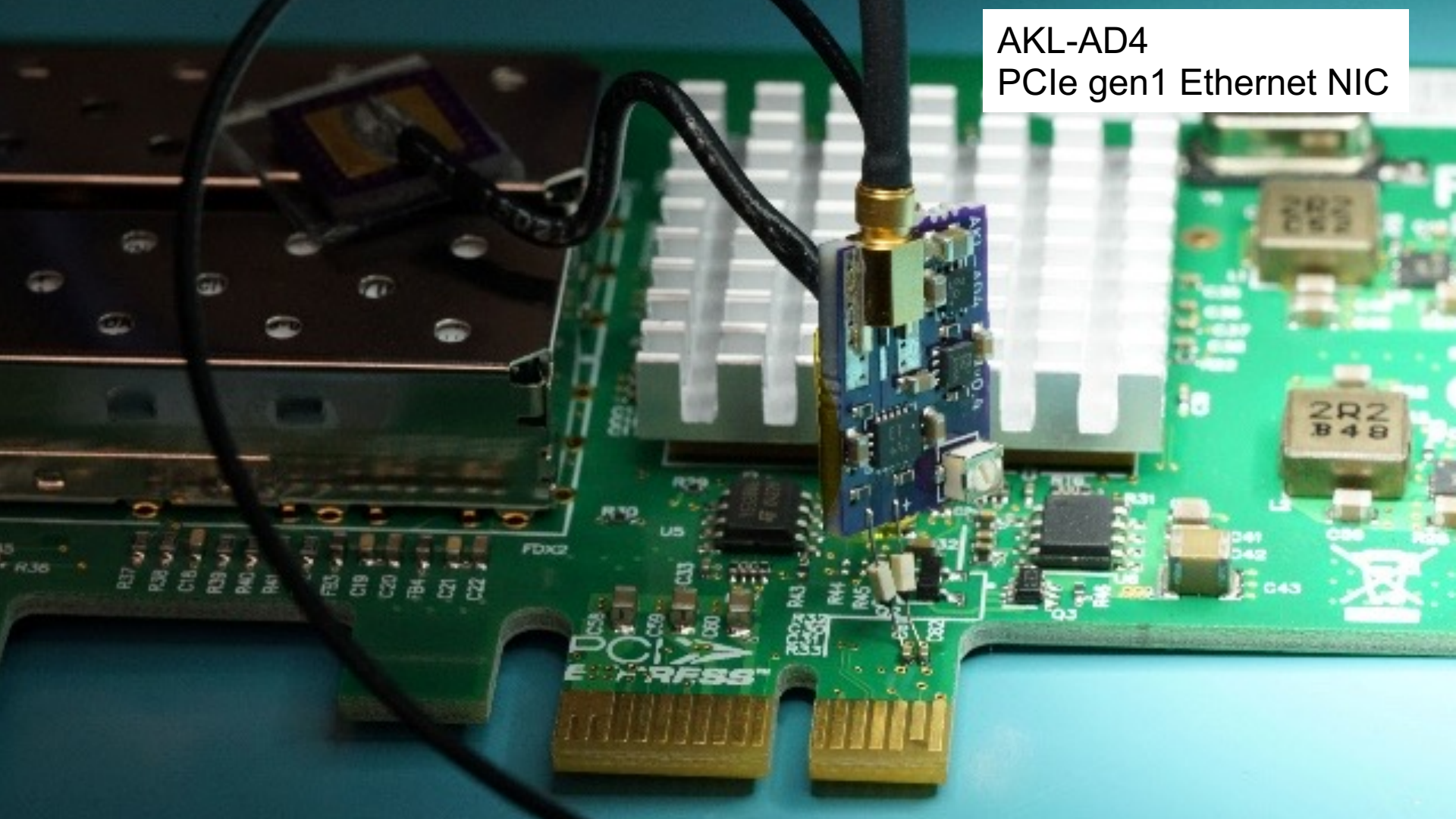
AKL-AD4
PCIe gen1 Ethernet NIC

AKL-PR1

- 10MΩ || 9.5 pF passive R-C divider probe
- Low cost, high density probing for low data rates
- Works with cheap scopes that only have 1MΩ inputs
- Early stage WIP (~200 MHz), working on more BW

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Software Stack

- `libscopehal`: instrument driver abstraction
- `libscopeprotocols`: Decodes / math blocks
- `glscopeclient`: Mature GTK based GUI
- `ngscopeclient`: Next-gen all-Vulkan GUI (WIP)
- Industry-friendly 3-clause BSD license

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Supported scopes (partial list)

- Digilent Analog Discovery family
- PicoScope 3000/6000 series
- R&S RTO6 series (also RTP? Same SW platform)
- Tek MSO 4/5/6 series
- Teledyne LeCroy MAUI platform
- Siglent SDS2000/5000/6000 series
- ThunderScope (not yet released)

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Filter graph model

- If you've used GNU Radio this should be familiar
- Chain source/sinks and processing blocks
- Multithreaded, GPU accelerated execution

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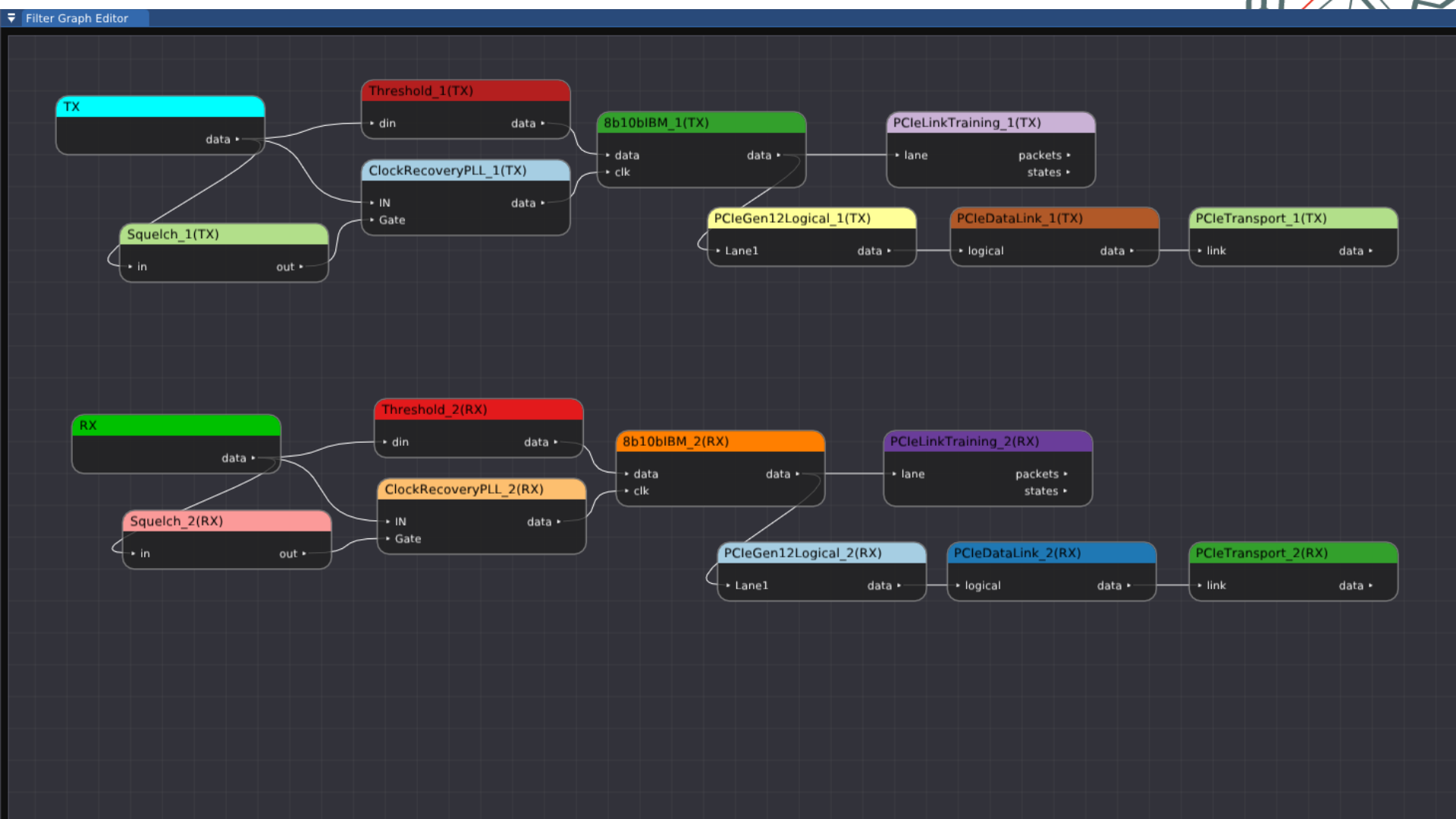
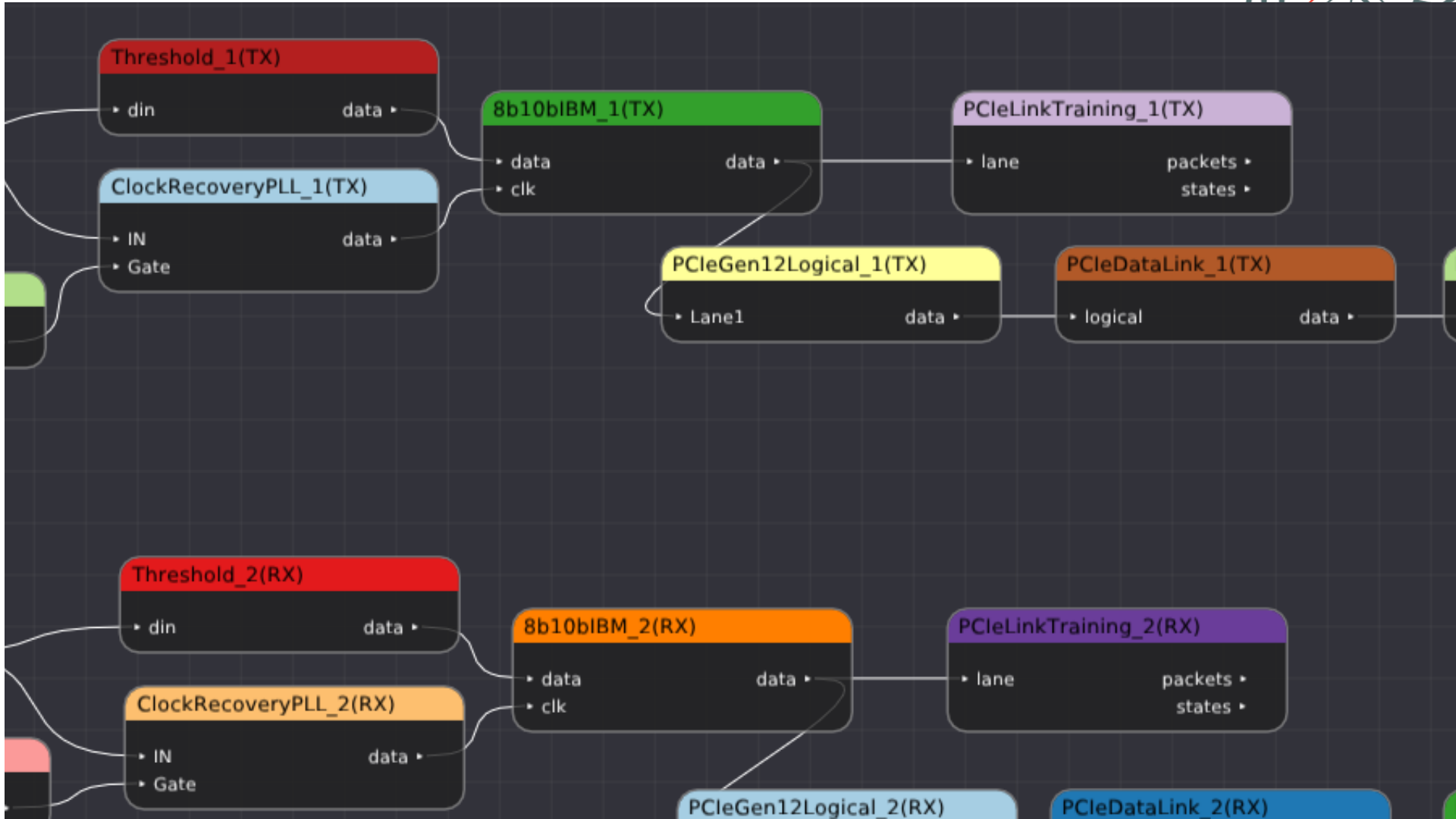
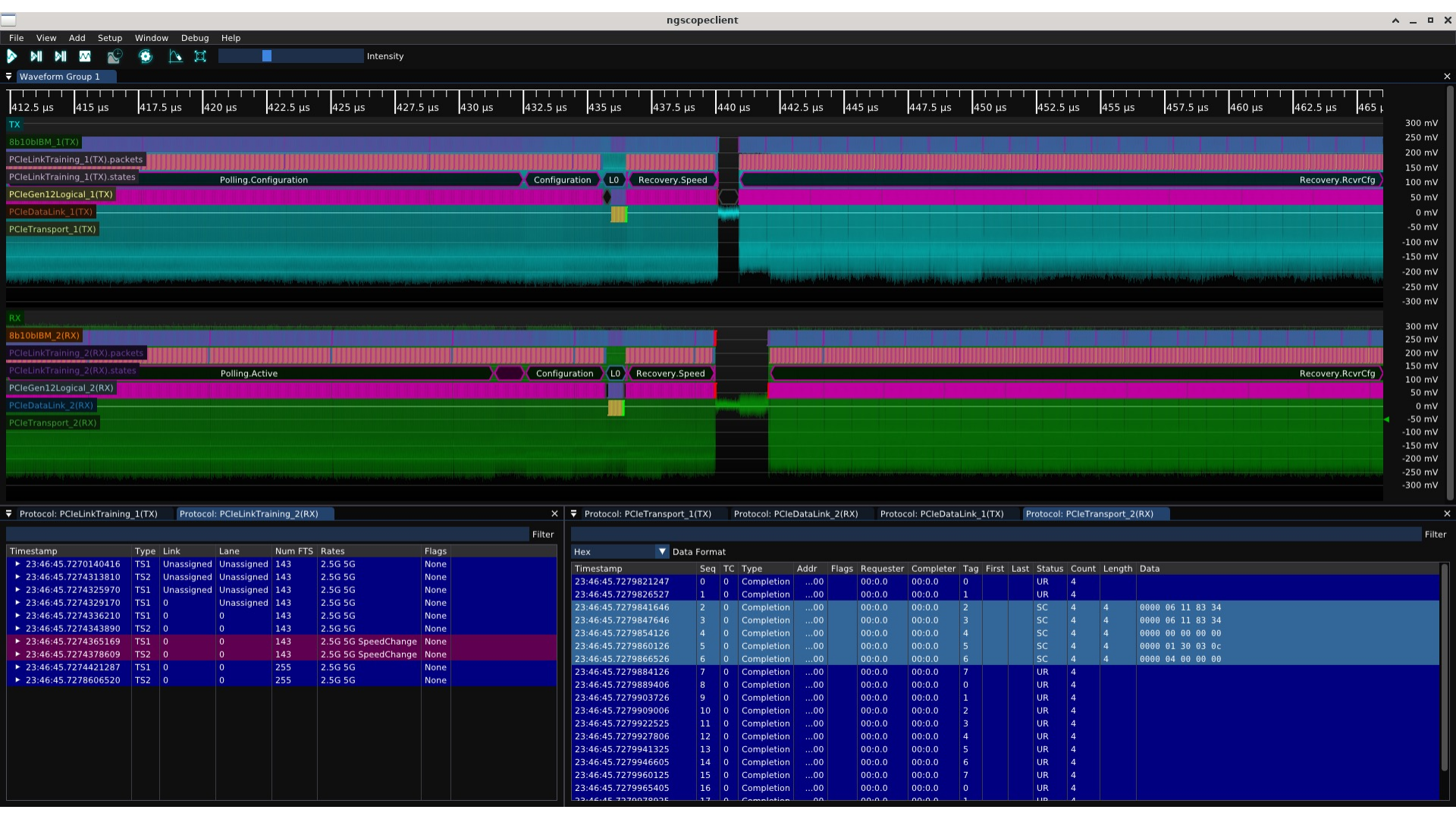
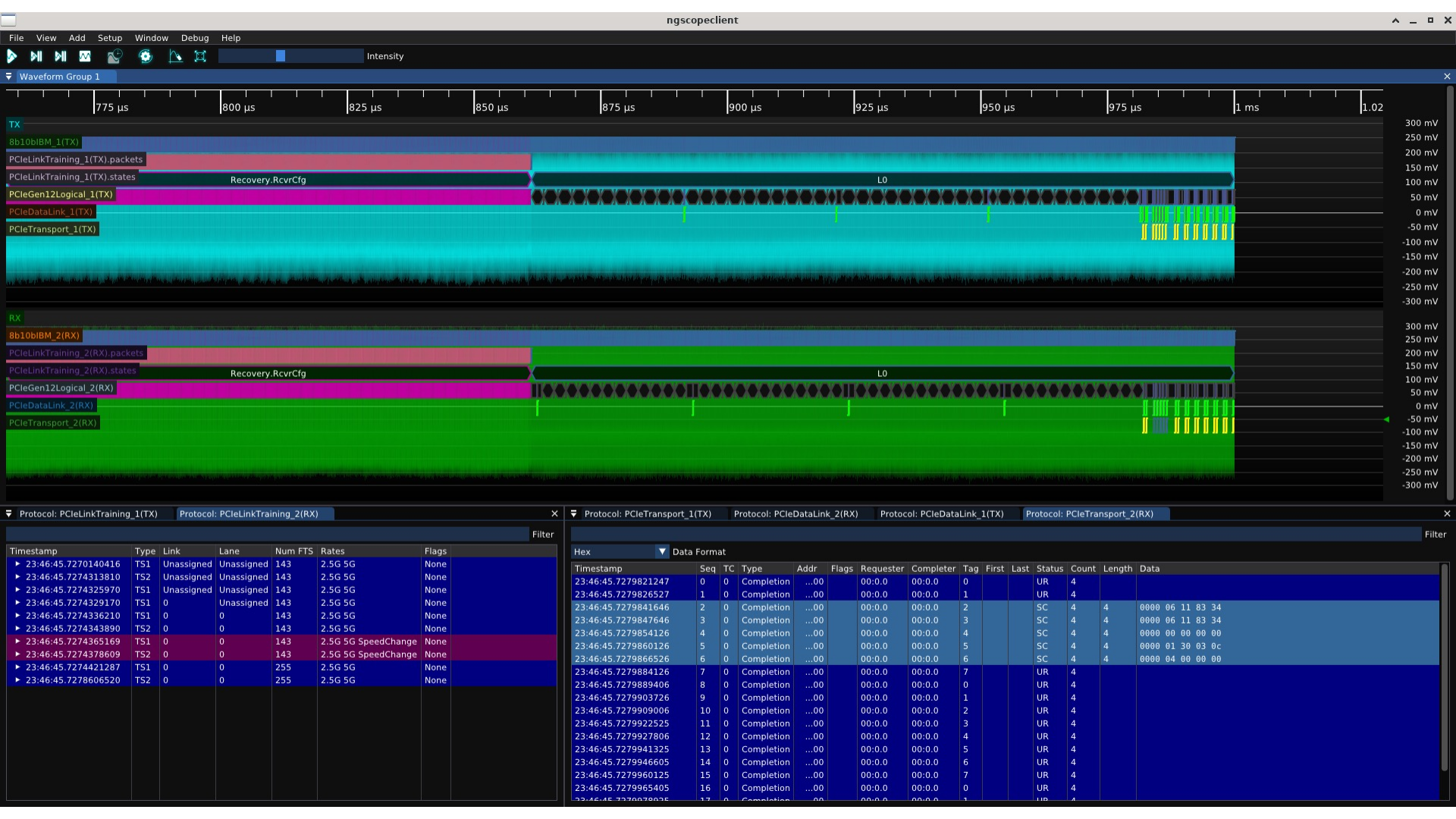

Filter Graph Editor
TX
data
Threshold_1(TX)
din
data
8b10bIBM_1(TX)
data
clk
data
PCIeLinkTraining_1(TX)
lane
packets
states
ClockRecoveryPLL_1(TX)
IN
Gate
data
Squelch_1(TX)
in
out
PCIeGen12Logical_1(TX)
Lane1
data
PCIeDataLink_1(TX)
logical
data
PCIeTransport_1(TX)
link
data
RX
data
Threshold_2(RX)
din
data
8b10bIBM_2(RX)
data
clk
data
PCIeLinkTraining_2(RX)
lane
packets
states
ClockRecoveryPLL_2(RX)
IN
Gate
data
Squelch_2(RX)
in
out
PCIeGen12Logical_2(RX)
Lane1
data
PCIeDataLink_2(RX)
logical
data
PCIeTransport_2(RX)
link
data


Threshold_1(TX)
din
data
8b10bIBM_1(TX)
data
clk
data
PCIeLinkTraining_1(TX)
lane
packets
states
ClockRecoveryPLL_1(TX)
IN
Gate
data
PCIeGen12Logical_1(TX)
Lane1
data
PCIeDataLink_1(TX)
logical
data
Threshold_2(RX)
din
data
8b10bIBM_2(RX)
data
clk
data
PCIeLinkTraining_2(RX)
lane
packets
states
ClockRecoveryPLL_2(RX)
IN
Gate
data
PCIeGen12Logical_2(RX)
PCIeDataLink_2(RX)


ngscopeclient
File View Add Setup Window Debug Help
Intensity
Waveform Group 1
412.5 µs 415 µs 417.5 µs 420 µs 422.5 µs 425 µs 427.5 µs 430 µs 432.5 µs 435 µs 437.5 µs 440 µs 442.5 µs 445 µs 447.5 µs 450 µs 452.5 µs 455 µs 457.5 µs 460 µs 462.5 µs 465 µs
TX
8b10bIBM_1(TX)
PCIeLinkTraining_1(TX).packets
PCIeLinkTraining_1(TX).states
Polling.Configuration
Configuration
L0
Recovery.Speed
Recovery.RcvrCfg
PCIeGen12Logical_1(TX)
PCIeDataLink_1(TX)
PCIeTransport_1(TX)
RX
8b10bIBM_2(RX)
PCIeLinkTraining_2(RX).packets
PCIeLinkTraining_2(RX).states
Polling.Active
Configuration
L0
Recovery.Speed
Recovery.RcvrCfg
PCIeGen12Logical_2(RX)
PCIeDataLink_2(RX)
PCIeTransport_2(RX)
300 mV 250 mV 200 mV 150 mV 100 mV 50 mV 0 mV -50 mV -100 mV -150 mV -200 mV -250 mV -300 mV
Protocol: PCIeLinkTraining_1(TX)
Protocol: PCIeLinkTraining_2(RX)
Filter
Timestamp Type Link Lane Num FTS Rates Flags
23:46:45.7270140416 TS1 Unassigned Unassigned 143 2.5G 5G None
23:46:45.7274313810 TS2 Unassigned Unassigned 143 2.5G 5G None
23:46:45.7274325970 TS1 Unassigned Unassigned 143 2.5G 5G None
23:46:45.7274329170 TS1 0 Unassigned 143 2.5G 5G None
23:46:45.7274336210 TS1 0 0 143 2.5G 5G None
23:46:45.7274343890 TS2 0 0 143 2.5G 5G None
23:46:45.7274365169 TS1 0 0 143 2.5G 5G SpeedChange None
23:46:45.7274378609 TS2 0 0 143 2.5G 5G SpeedChange None
23:46:45.7274421287 TS1 0 0 255 2.5G 5G None
23:46:45.7278606520 TS2 0 0 255 2.5G 5G None
Protocol: PCIeTransport_1(TX)
Protocol: PCIeDataLink_2(RX)
Protocol: PCIeDataLink_1(TX)
Protocol: PCIeTransport_2(RX)
Filter
Hex
Data Format
Timestamp Seq TC Type Addr Flags Requester Completer Tag First Last Status Count Length Data
23:46:45.7279821247 0 0 Completion ...00 00:0.0 00:0.0 0 UR 4
23:46:45.7279826527 1 0 Completion ...00 00:0.0 00:0.0 1 UR 4
23:46:45.7279841646 2 0 Completion ...00 00:0.0 00:0.0 2 SC 4 4 0000 06 11 83 34
23:46:45.7279847646 3 0 Completion ...00 00:0.0 00:0.0 3 SC 4 4 0000 06 11 83 34
23:46:45.7279854126 4 0 Completion ...00 00:0.0 00:0.0 4 SC 4 4 0000 00 00 00 00
23:46:45.7279860126 5 0 Completion ...00 00:0.0 00:0.0 5 SC 4 4 0000 01 30 03 0c
23:46:45.7279866526 6 0 Completion ...00 00:0.0 00:0.0 6 SC 4 4 0000 04 00 00 00
23:46:45.7279884126 7 0 Completion ...00 00:0.0 00:0.0 7 UR 4
23:46:45.7279889406 8 0 Completion ...00 00:0.0 00:0.0 0 UR 4
23:46:45.7279903726 9 0 Completion ...00 00:0.0 00:0.0 1 UR 4
23:46:45.7279909006 10 0 Completion ...00 00:0.0 00:0.0 2 UR 4
23:46:45.7279922525 11 0 Completion ...00 00:0.0 00:0.0 3 UR 4
23:46:45.7279927806 12 0 Completion ...00 00:0.0 00:0.0 4 UR 4
23:46:45.7279941325 13 0 Completion ...00 00:0.0 00:0.0 5 UR 4
23:46:45.7279946605 14 0 Completion ...00 00:0.0 00:0.0 6 UR 4
23:46:45.7279960125 15 0 Completion ...00 00:0.0 00:0.0 7 UR 4
23:46:45.7279965405 16 0 Completion ...00 00:0.0 00:0.0 0 UR 4


ngscopeclient
File View Add Setup Window Debug Help
Intensity
Waveform Group 1
775 µs
800 µs
825 µs
850 µs
875 µs
900 µs
925 µs
950 µs
975 µs
1 ms
1.02
TX
8b10bIBM_1(TX)
PCIeLinkTraining_1(TX).packets
PCIeLinkTraining_1(TX).states
Recovery.RcvrCfg
L0
PCIeGen12Logical_1(TX)
PCIeDataLink_1(TX)
PCIeTransport_1(TX)
RX
8b10bIBM_2(RX)
PCIeLinkTraining_2(RX).packets
PCIeLinkTraining_2(RX).states
Recovery.RcvrCfg
L0
PCIeGen12Logical_2(RX)
PCIeDataLink_2(RX)
PCIeTransport_2(RX)
300 mV
250 mV
200 mV
150 mV
100 mV
50 mV
0 mV
-50 mV
-100 mV
-150 mV
-200 mV
-250 mV
-300 mV
Protocol: PCIeLinkTraining_1(TX)
Protocol: PCIeLinkTraining_2(RX)
Filter
Timestamp Type Link Lane Num FTS Rates Flags
23:46:45.7270140416 TS1 Unassigned Unassigned 143 2.5G 5G None
23:46:45.7274313810 TS2 Unassigned Unassigned 143 2.5G 5G None
23:46:45.7274325970 TS1 Unassigned Unassigned 143 2.5G 5G None
23:46:45.7274329170 TS1 0 Unassigned 143 2.5G 5G None
23:46:45.7274336210 TS1 0 0 143 2.5G 5G None
23:46:45.7274343890 TS2 0 0 143 2.5G 5G None
23:46:45.7274365169 TS1 0 0 143 2.5G 5G SpeedChange None
23:46:45.7274378609 TS2 0 0 143 2.5G 5G SpeedChange None
23:46:45.7274421287 TS1 0 0 255 2.5G 5G None
23:46:45.7278606520 TS2 0 0 255 2.5G 5G None
Protocol: PCIeTransport_1(TX)
Protocol: PCIeDataLink_2(RX)
Protocol: PCIeDataLink_1(TX)
Protocol: PCIeTransport_2(RX)
Filter
Hex
Data Format
Timestamp Seq TC Type Addr Flags Requester Completer Tag First Last Status Count Length Data
23:46:45.7279821247 0 0 Completion ...00 00:0.0 00:0.0 0 UR 4
23:46:45.7279826527 1 0 Completion ...00 00:0.0 00:0.0 1 UR 4
23:46:45.7279841646 2 0 Completion ...00 00:0.0 00:0.0 2 SC 4 4 0000 06 11 83 34
23:46:45.7279847646 3 0 Completion ...00 00:0.0 00:0.0 3 SC 4 4 0000 06 11 83 34
23:46:45.7279854126 4 0 Completion ...00 00:0.0 00:0.0 4 SC 4 4 0000 00 00 00 00
23:46:45.7279860126 5 0 Completion ...00 00:0.0 00:0.0 5 SC 4 4 0000 01 30 03 0c
23:46:45.7279866526 6 0 Completion ...00 00:0.0 00:0.0 6 SC 4 4 0000 04 00 00 00
23:46:45.7279884126 7 0 Completion ...00 00:0.0 00:0.0 7 UR 4
23:46:45.7279889406 8 0 Completion ...00 00:0.0 00:0.0 0 UR 4
23:46:45.7279903726 9 0 Completion ...00 00:0.0 00:0.0 1 UR 4
23:46:45.7279909006 10 0 Completion ...00 00:0.0 00:0.0 2 UR 4
23:46:45.7279922525 11 0 Completion ...00 00:0.0 00:0.0 3 UR 4
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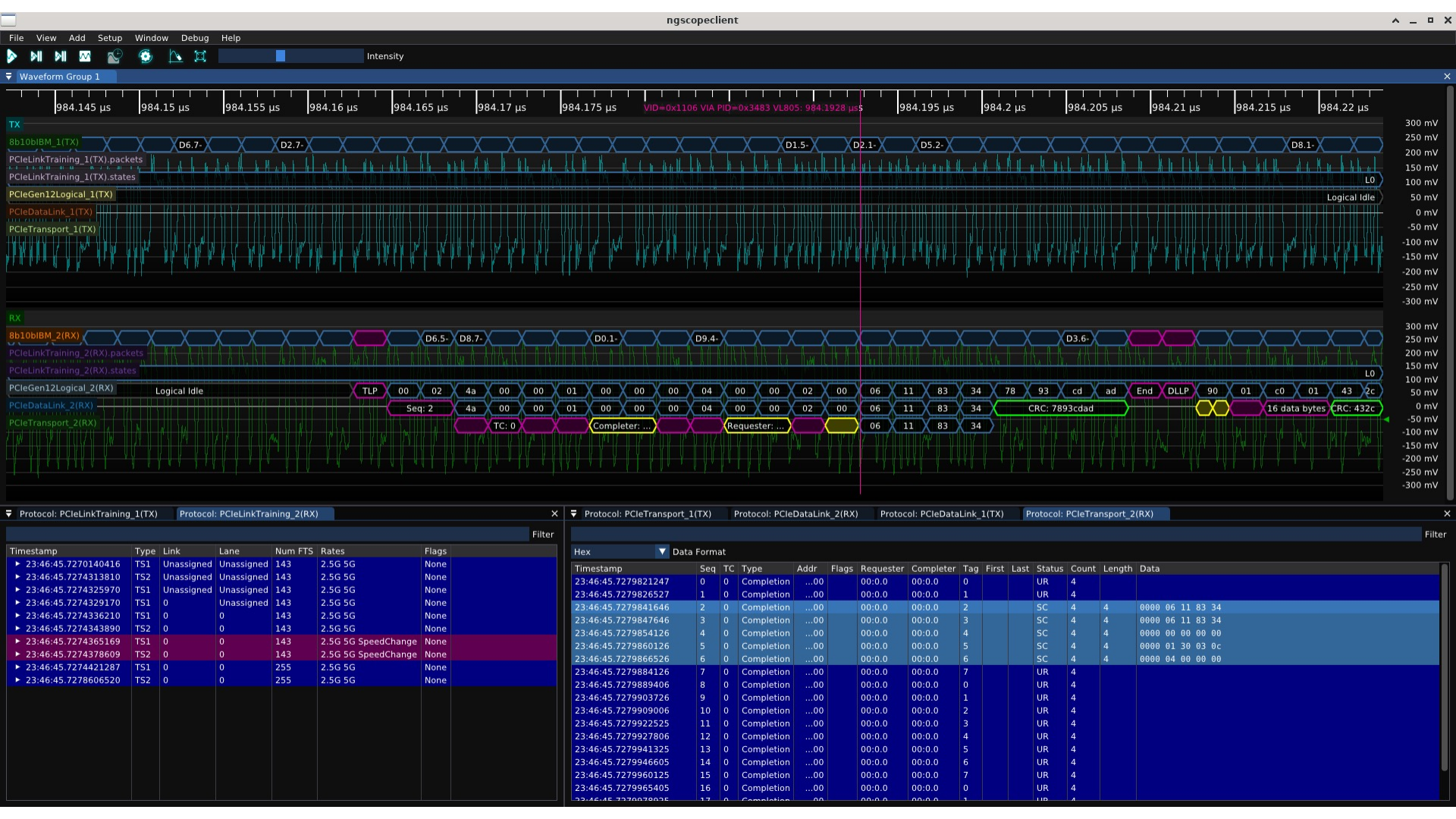
23:46:45.7279941325 13 0 Completion ...00 00:0.0 00:0.0 5 UR 4
23:46:45.7279946605 14 0 Completion ...00 00:0.0 00:0.0 6 UR 4
23:46:45.7279960125 15 0 Completion ...00 00:0.0 00:0.0 7 UR 4
23:46:45.7279965405 16 0 Completion ...00 00:0.0 00:0.0 0 UR 4


ngscopeclient
File View Add Setup Window Debug Help
Intensity
Waveform Group 1
984.145 µs 984.15 µs 984.155 µs 984.16 µs 984.165 µs 984.17 µs 984.175 µs
VID=0x1106 VIA PID=0x3483 VL805: 984.1928 µs
984.195 µs 984.2 µs 984.205 µs 984.21 µs 984.215 µs 984.22 µs
TX
8b10bIBM_1(TX)
D6.7- D2.7- D1.5- D2.1- D5.2- D8.1-
PCIeLinkTraining_1(TX).packets
PCIeLinkTraining_1(TX).states
L0
PCIeGen12Logical_1(TX)
Logical Idle
PCIeDataLink_1(TX)
PCIeTransport_1(TX)
300 mV 250 mV 200 mV 150 mV 100 mV 50 mV 0 mV -50 mV -100 mV -150 mV -200 mV -250 mV -300 mV
RX
8b10bIBM_2(RX)
D6.5- D8.7- D0.1- D9.4- D3.6-
PCIeLinkTraining_2(RX).packets
PCIeLinkTraining_2(RX).states
L0
PCIeGen12Logical_2(RX)
Logical Idle
TLP 00 02 4a 00 00 01 00 00 00 04 00 00 02 00 06 11 83 34 78 93 cd ad End DLLP 90 01 c0 01 43 2c
PCIeDataLink_2(RX)
Seq: 2 4a 00 00 01 00 00 00 04 00 00 02 00 06 11 83 34 CRC: 7893cdad 16 data bytes CRC: 432c
PCIeTransport_2(RX)
TC: 0 Completer: ... Requester: ... 06 11 83 34
300 mV 250 mV 200 mV 150 mV 100 mV 50 mV 0 mV -50 mV -100 mV -150 mV -200 mV -250 mV -300 mV
Protocol: PCIeLinkTraining_1(TX)
Protocol: PCIeLinkTraining_2(RX)
Filter
Timestamp Type Link Lane Num FTS Rates Flags
23:46:45.7270140416 TS1 Unassigned Unassigned 143 2.5G 5G None
23:46:45.7274313810 TS2 Unassigned Unassigned 143 2.5G 5G None
23:46:45.7274325970 TS1 Unassigned Unassigned 143 2.5G 5G None
23:46:45.7274329170 TS1 0 Unassigned 143 2.5G 5G None
23:46:45.7274336210 TS1 0 0 143 2.5G 5G None
23:46:45.7274343890 TS2 0 0 143 2.5G 5G None
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23:46:45.7274378609 TS2 0 0 143 2.5G 5G SpeedChange None
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Protocol: PCIeTransport_1(TX)
Protocol: PCIeDataLink_2(RX)
Protocol: PCIeDataLink_1(TX)
Protocol: PCIeTransport_2(RX)
Filter
Hex
Data Format
Timestamp Seq TC Type Addr Flags Requester Completer Tag First Last Status Count Length Data
23:46:45.7279821247 0 0 Completion ...00 00:0.0 00:0.0 0 UR 4
23:46:45.7279826527 1 0 Completion ...00 00:0.0 00:0.0 1 UR 4
23:46:45.7279841646 2 0 Completion ...00 00:0.0 00:0.0 2 SC 4 4 0000 06 11 83 34
23:46:45.7279847646 3 0 Completion ...00 00:0.0 00:0.0 3 SC 4 4 0000 06 11 83 34
23:46:45.7279854126 4 0 Completion ...00 00:0.0 00:0.0 4 SC 4 4 0000 00 00 00 00
23:46:45.7279860126 5 0 Completion ...00 00:0.0 00:0.0 5 SC 4 4 0000 01 30 03 0c
23:46:45.7279866526 6 0 Completion ...00 00:0.0 00:0.0 6 SC 4 4 0000 04 00 00 00
23:46:45.7279884126 7 0 Completion ...00 00:0.0 00:0.0 7 UR 4
23:46:45.7279889406 8 0 Completion ...00 00:0.0 00:0.0 0 UR 4
23:46:45.7279903726 9 0 Completion ...00 00:0.0 00:0.0 1 UR 4
23:46:45.7279909006 10 0 Completion ...00 00:0.0 00:0.0 2 UR 4
23:46:45.7279922525 11 0 Completion ...00 00:0.0 00:0.0 3 UR 4
23:46:45.7279927806 12 0 Completion ...00 00:0.0 00:0.0 4 UR 4
23:46:45.7279941325 13 0 Completion ...00 00:0.0 00:0.0 5 UR 4
23:46:45.7279946605 14 0 Completion ...00 00:0.0 00:0.0 6 UR 4
23:46:45.7279960125 15 0 Completion ...00 00:0.0 00:0.0 7 UR 4
23:46:45.7279965405 16 0 Completion ...00 00:0.0 00:0.0 0 UR 4

Protocol: PCIeTransport_1(TX) | Protocol: PCIeDataLink_2(RX) | Protocol: PCIeDataLink_1(TX) | Protocol: PCIeTransport_2(RX)

Filter

Hex ▼ Data Format

Timestamp	Seq	TC	Type	Addr	Flags	Requester	Completer	Tag	First	Last	Status	Count	Length	Data
23:46:45.7279821247	0	0	Completion	...00		00:0.0	00:0.0	0			UR	4		
23:46:45.7279826527	1	0	Completion	...00		00:0.0	00:0.0	1			UR	4		
23:46:45.7279841646	2	0	Completion	...00		00:0.0	00:0.0	2			SC	4	4	0000 06 11 83 34
23:46:45.7279847646	3	0	Completion	...00		00:0.0	00:0.0	3			SC	4	4	0000 06 11 83 34
23:46:45.7279854126	4	0	Completion	...00		00:0.0	00:0.0	4			SC	4	4	0000 00 00 00 00
23:46:45.7279860126	5	0	Completion	...00		00:0.0	00:0.0	5			SC	4	4	0000 01 30 03 0c
23:46:45.7279866526	6	0	Completion	...00		00:0.0	00:0.0	6			SC	4	4	0000 04 00 00 00
23:46:45.7279884126	7	0	Completion	...00		00:0.0	00:0.0	7			UR	4		

Supported protocols (partial list)

- 10baseT / 100baseTX
- 1000baseX
- 10Gbase-R
- 8b/10b
- 64b/66b
- CAN
- DDR 1/3 cmd bus
- I2C
- I2C EEPROM
- Intel eSPI
- *MII
- MIL-STD-1553
- MIPI D-PHY, DSI
- PCIe gen 1/2/3 (4/5?)
- [Q]SPI
- Serial flash
- UART
- USB LS/FS/HS
- And more (150+)

IOActive™

DSP / SI capabilities

- Eye pattern
- FIR filters
- FFT / spectrogram
- Jitter decomposition / spectrum
- S-parameter cascade / de-embed (no AFR… yet)
- Time domain S-param channel emulation / de-embed

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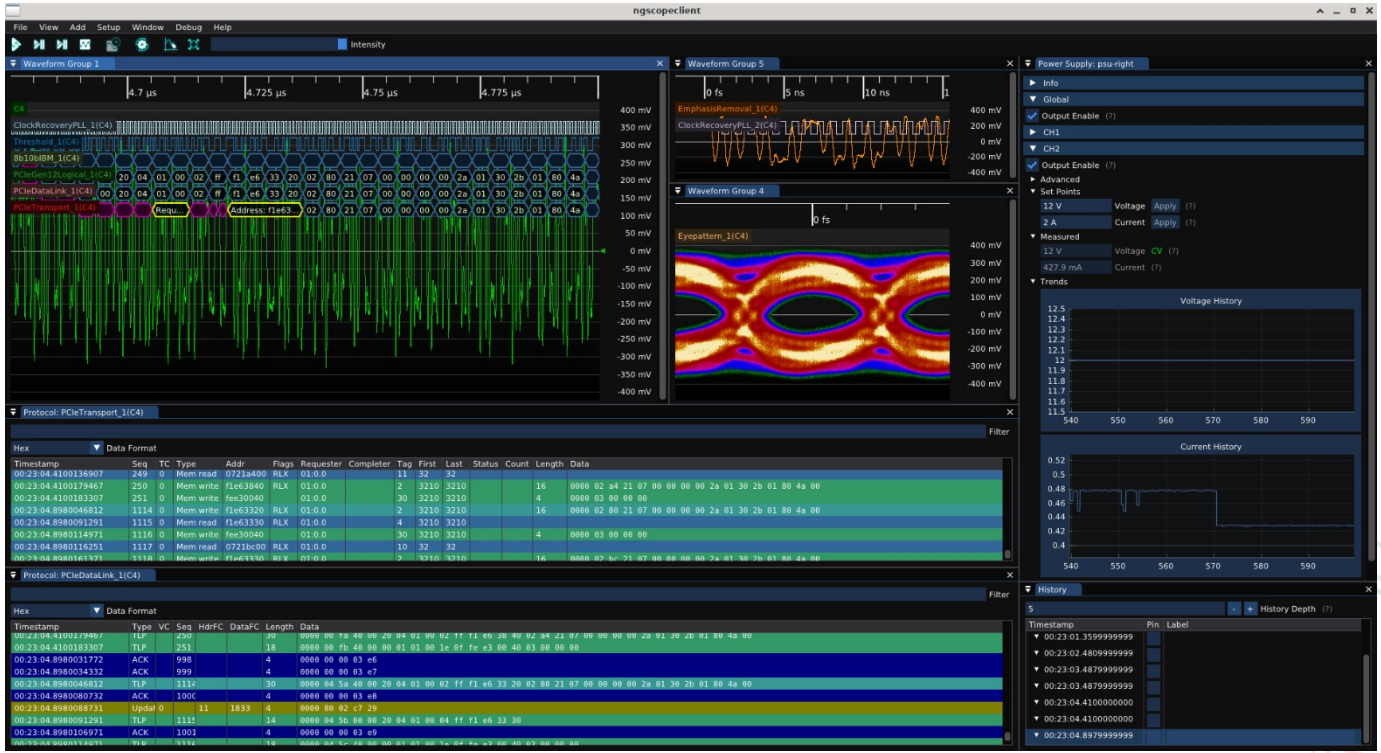
PCIe protocol decode + SI



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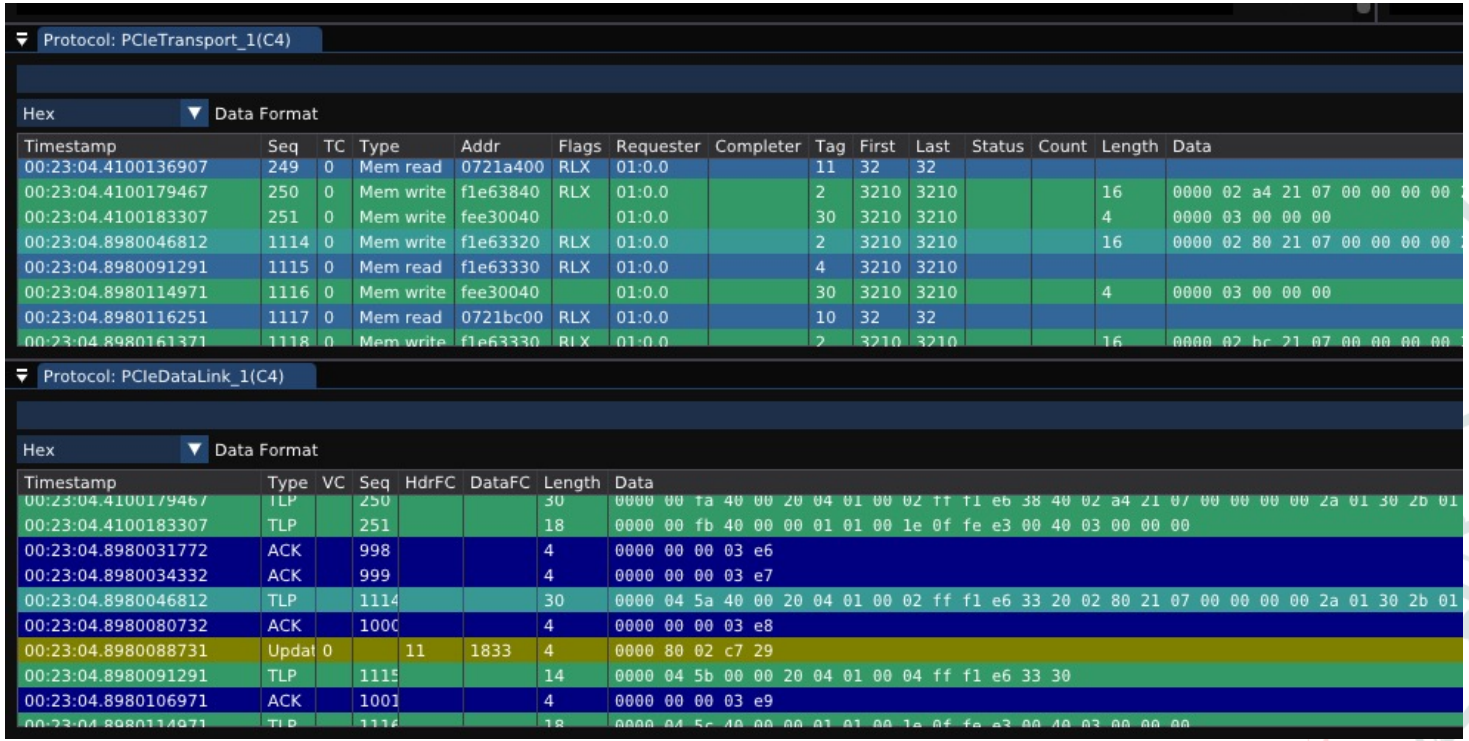
PCIe protocol decode



Protocol: PCIeTransport_1(C4)

Hex ▼ Data Format

Timestamp	Seq	TC	Type	Addr	Flags	Requester	Completer	Tag	First	Last	Status	Count	Length	Data
00:23:04.4100136907	249	0	Mem read	0721a400	RLX	01:0.0		11	32	32				
00:23:04.4100179467	250	0	Mem write	f1e63840	RLX	01:0.0		2	3210	3210			16	0000 02 a4 21 07 00 00 00 00
00:23:04.4100183307	251	0	Mem write	fee30040		01:0.0		30	3210	3210			4	0000 03 00 00 00
00:23:04.8980046812	1114	0	Mem write	f1e63320	RLX	01:0.0		2	3210	3210			16	0000 02 80 21 07 00 00 00 00
00:23:04.8980091291	1115	0	Mem read	f1e63330	RLX	01:0.0		4	3210	3210				
00:23:04.8980114971	1116	0	Mem write	fee30040		01:0.0		30	3210	3210			4	0000 03 00 00 00
00:23:04.8980116251	1117	0	Mem read	0721bc00	RLX	01:0.0		10	32	32				
00:23:04.8980161371	1118	0	Mem write	f1e63330	RLX	01:0.0		2	3210	3210			16	0000 02 bc 21 07 00 00 00 00

Protocol: PCIeDataLink_1(C4)

Hex ▼ Data Format

Timestamp	Type	VC	Seq	HdrFC	DataFC	Length	Data
00:23:04.4100179467	TLP		250			30	0000 00 fa 40 00 20 04 01 00 02 ff f1 e6 38 40 02 a4 21 07 00 00 00 00 2a 01 30 2b 01
00:23:04.4100183307	TLP		251			18	0000 00 fb 40 00 00 01 01 00 1e 0f fe e3 00 40 03 00 00 00
00:23:04.8980031772	ACK		998			4	0000 00 00 03 e6
00:23:04.8980034332	ACK		999			4	0000 00 00 03 e7
00:23:04.8980046812	TLP		1114			30	0000 04 5a 40 00 20 04 01 00 02 ff f1 e6 33 20 02 80 21 07 00 00 00 00 2a 01 30 2b 01
00:23:04.8980080732	ACK		1000			4	0000 00 00 03 e8
00:23:04.8980088731	Updat	0		11	1833	4	0000 80 02 c7 29
00:23:04.8980091291	TLP		1115			14	0000 04 5b 00 00 20 04 01 00 04 ff f1 e6 33 30
00:23:04.8980106971	ACK		1001			4	0000 00 00 03 e9
00:23:04.8980114971	TLP		1116			18	0000 04 5c 40 00 00 01 01 00 1e 0f fe e3 00 40 03 00 00 00

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Extensibility

- Decodes and drivers are single C++ classes
  - Can be in main codebase or a plugin
- New decodes can layer on / fork any existing one
- Recent real-world examples:
  - Proprietary framing over 64b/66b
  - Proprietary upper layer over SATA link layer
  - Custom firmware speaking I2C
  - 1-Wire with slightly out of spec timing
  - SPA on PCIe device w/ TLP trigger

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Multi instrument capability

- Can interface with more than scopes!
  - Multimeters
  - Power supplies
  - RF signal generators
  - Function generators
  - (WIP) VNAs
- Can connect to multiple scopes simultaneously
  - Cross trigger cascade w/ calibrated delay

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Multi scope case study

- 10 Gbps retimer with I2C management interface
  - 5 OOM difference in data rates!
- Some management commands cause dropouts
- We want to study this in more detail

Multi scope case study

- Obvious option: fast scope w/ 2G points of memory
  - But where do you find this?
  - My SDA is 128M points. Even LabMaster is only 1.5G
- Better option: Fast scope and slow scope
  - Teledyne LeCroy SDA 816Zi (2 MS @ 40 Gsps)
  - PicoScope 6824E (20 MS @ 312.5 Msps)
  - “Only” 2 OOM diff in sample rates for this demo
  - 312 Msps is overkill for I2C, could go much slower

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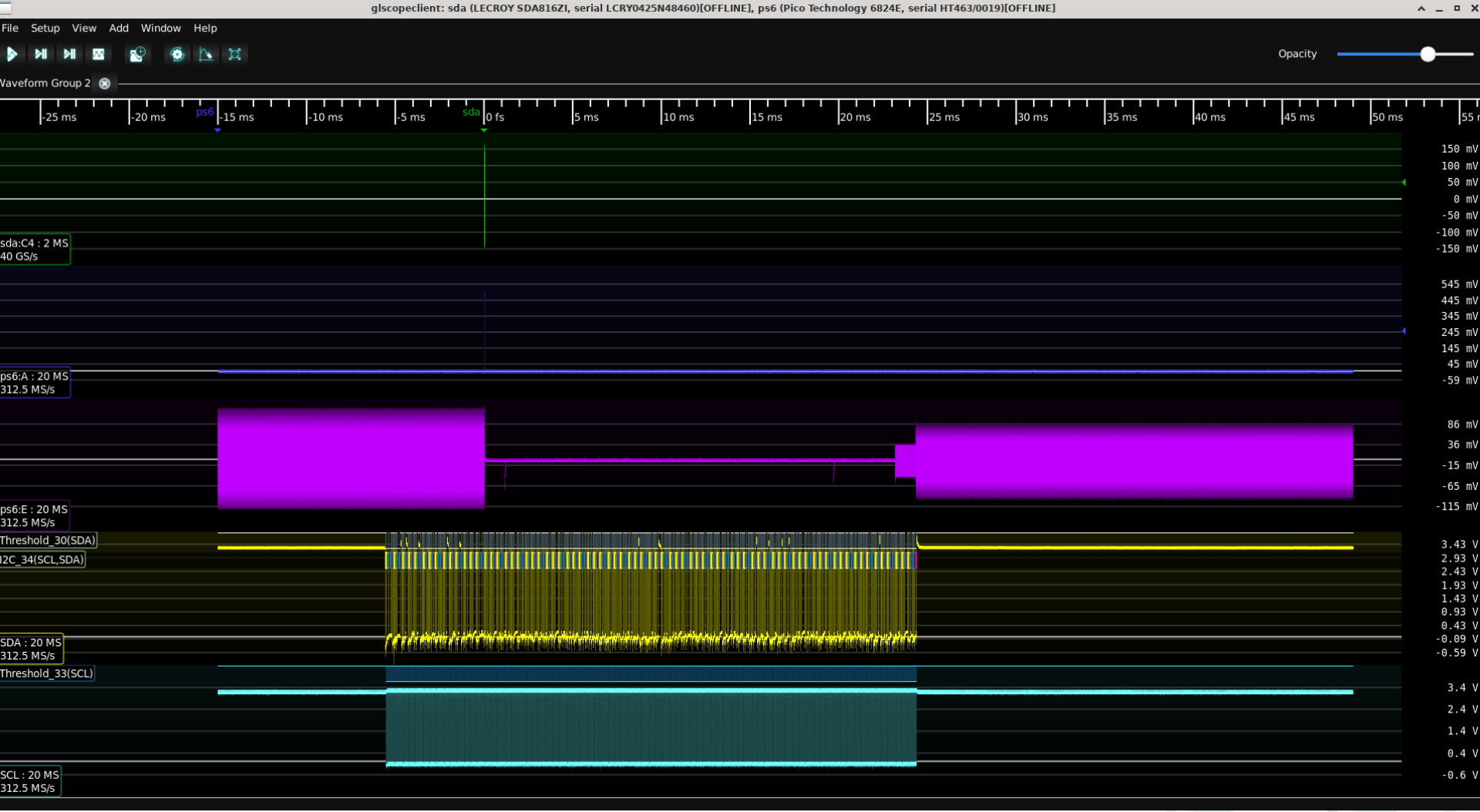
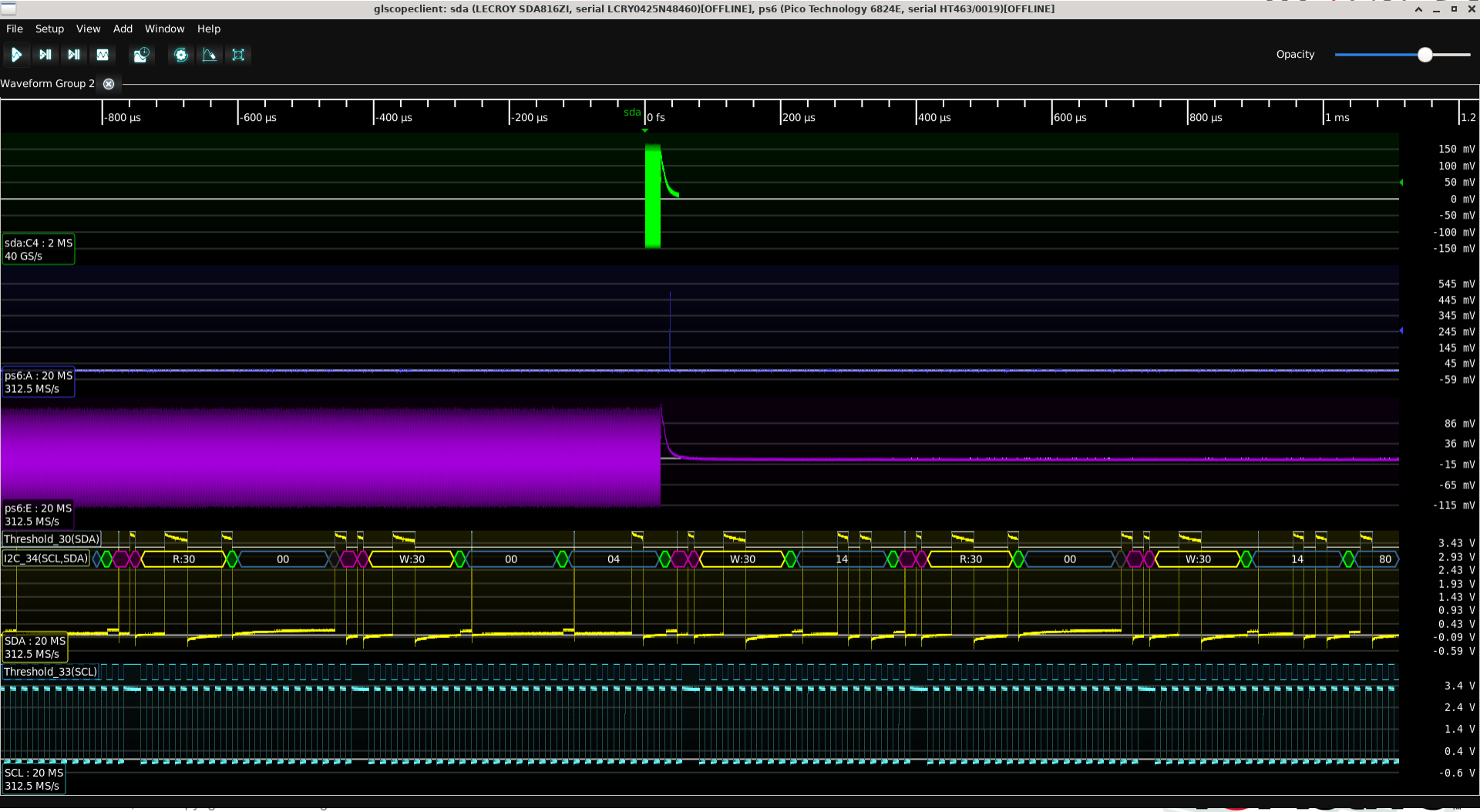
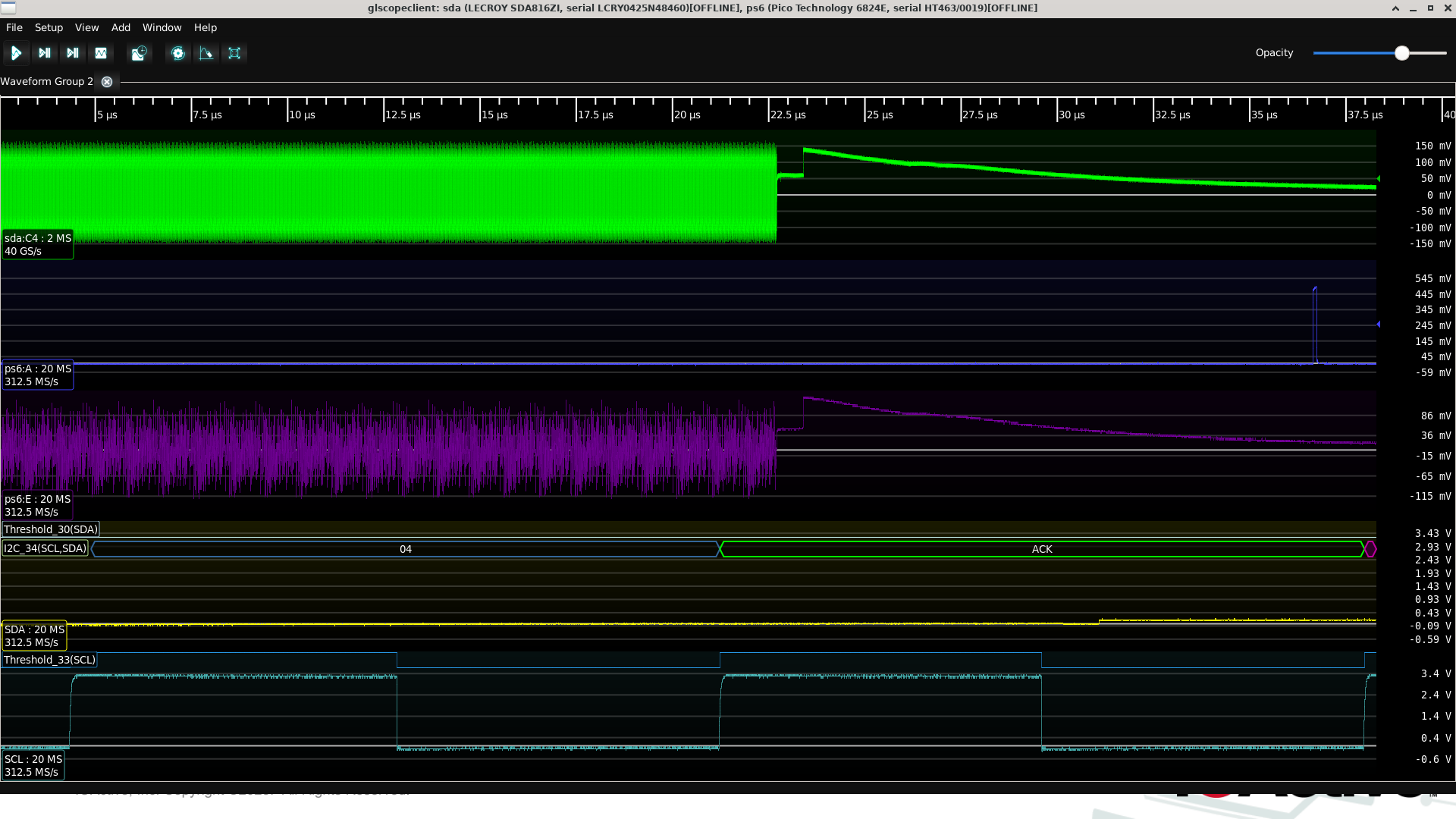
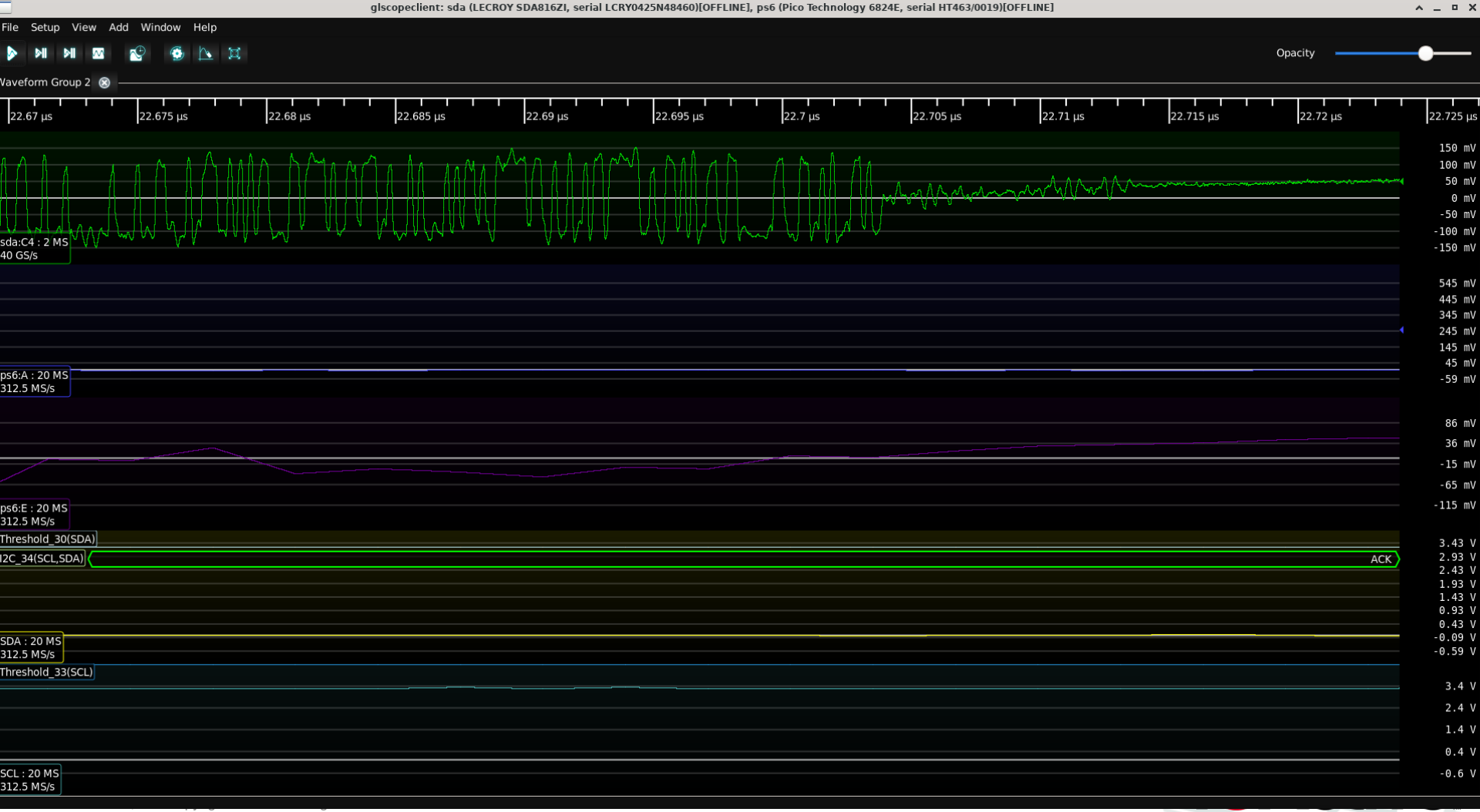

glscopeclient: sda (LECROY SDA816ZI, serial LCRY0425N48460)[OFFLINE], ps6 (Pico Technology 6824E, serial HT463/0019)[OFFLINE]
File
Setup
View
Add
Window
Help
Opacity
Waveform Group 2
-25 ms
-20 ms
ps6
-15 ms
-10 ms
-5 ms
sda
0 fs
5 ms
10 ms
15 ms
20 ms
25 ms
30 ms
35 ms
40 ms
45 ms
50 ms
sda:C4 : 2 MS
40 GS/s
150 mV
100 mV
50 mV
0 mV
-50 mV
-100 mV
-150 mV
ps6:A : 20 MS
312.5 MS/s
545 mV
445 mV
345 mV
245 mV
145 mV
45 mV
-59 mV
ps6:E : 20 MS
312.5 MS/s
86 mV
36 mV
-15 mV
-65 mV
-115 mV
Threshold_30(SDA)
I2C_34(SCL,SDA)
3.43 V
2.93 V
2.43 V
1.93 V
1.43 V
0.93 V
0.43 V
-0.09 V
-0.59 V
SDA : 20 MS
312.5 MS/s
Threshold_33(SCL)
3.4 V
2.4 V
1.4 V
0.4 V
-0.6 V
SCL : 20 MS
312.5 MS/s


glscopeclient: sda (LECROY SDA816ZI, serial LCRY0425N48460)[OFFLINE], ps6 (Pico Technology 6824E, serial HT463/0019)[OFFLINE]
File
Setup
View
Add
Window
Help
Opacity
Waveform Group 2
-800 µs
-600 µs
-400 µs
-200 µs
sda
0 fs
200 µs
400 µs
600 µs
800 µs
1 ms
1.2
150 mV
100 mV
50 mV
0 mV
-50 mV
-100 mV
-150 mV
sda:C4 : 2 MS
40 GS/s
545 mV
445 mV
345 mV
245 mV
145 mV
45 mV
-59 mV
ps6:A : 20 MS
312.5 MS/s
86 mV
36 mV
-15 mV
-65 mV
-115 mV
ps6:E : 20 MS
312.5 MS/s
Threshold_30(SDA)
I2C_34(SCL,SDA)
R:30
00
W:30
00
04
W:30
14
R:30
00
W:30
14
80
3.43 V
2.93 V
2.43 V
1.93 V
1.43 V
0.93 V
0.43 V
-0.09 V
-0.59 V
SDA : 20 MS
312.5 MS/s
Threshold_33(SCL)
3.4 V
2.4 V
1.4 V
0.4 V
-0.6 V
SCL : 20 MS
312.5 MS/s


glscopeclient: sda (LECROY SDA816ZI, serial LCRY0425N48460)[OFFLINE], ps6 (Pico Technology 6824E, serial HT463/0019)[OFFLINE]
File
Setup
View
Add
Window
Help
Opacity
Waveform Group 2
5 µs
7.5 µs
10 µs
12.5 µs
15 µs
17.5 µs
20 µs
22.5 µs
25 µs
27.5 µs
30 µs
32.5 µs
35 µs
37.5 µs
150 mV
100 mV
50 mV
0 mV
-50 mV
-100 mV
-150 mV
sda:C4 : 2 MS
40 GS/s
545 mV
445 mV
345 mV
245 mV
145 mV
45 mV
-59 mV
ps6:A : 20 MS
312.5 MS/s
86 mV
36 mV
-15 mV
-65 mV
-115 mV
ps6:E : 20 MS
312.5 MS/s
Threshold_30(SDA)
3.43 V
2.93 V
2.43 V
1.93 V
1.43 V
0.93 V
0.43 V
-0.09 V
-0.59 V
I2C_34(SCL,SDA)
04
ACK
SDA : 20 MS
312.5 MS/s
Threshold_33(SCL)
3.4 V
2.4 V
1.4 V
0.4 V
-0.6 V
SCL : 20 MS
312.5 MS/s


glscopeclient: sda (LECROY SDA816ZI, serial LCRY0425N48460)[OFFLINE], ps6 (Pico Technology 6824E, serial HT463/0019)[OFFLINE]
File
Setup
View
Add
Window
Help
Opacity
Waveform Group 2
22.67 µs
22.675 µs
22.68 µs
22.685 µs
22.69 µs
22.695 µs
22.7 µs
22.705 µs
22.71 µs
22.715 µs
22.72 µs
22.725 µs
sda:C4 : 2 MS
40 GS/s
150 mV
100 mV
50 mV
0 mV
-50 mV
-100 mV
-150 mV
ps6:A : 20 MS
312.5 MS/s
545 mV
445 mV
345 mV
245 mV
145 mV
45 mV
-59 mV
ps6:E : 20 MS
312.5 MS/s
86 mV
36 mV
-15 mV
-65 mV
-115 mV
Threshold_30(SDA)
I2C_34(SCL,SDA)
ACK
3.43 V
2.93 V
2.43 V
1.93 V
1.43 V
0.93 V
0.43 V
SDA : 20 MS
312.5 MS/s
-0.09 V
-0.59 V
Threshold_33(SCL)
3.4 V
2.4 V
1.4 V
0.4 V
SCL : 20 MS
312.5 MS/s
-0.6 V

Questions?

- https://github.com/glscopeclient/scopehal-apps/

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